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Jameco Part Number 134181

PIC16C5X

EPROM/ROM-Based 8-Bit CMOS Microcontroller Series

Devices Included in this Data Sheet:

- PIC16C54
- PIC16CR54
- PIC16C55
- PIC16C56
- PIC16CR56
- PIC16C57
- PIC16CR57
- PIC16C58
- PIC16CR58

Note: 16C5X refers to all revisions of the part (i.e., 16C54 refers to 16C54, 16C54A, and 16C54C), unless specifically called out otherwise.

High-Performance RISC CPU:

- Only 33 single word instructions to learn
- All instructions are single cycle (200 ns) except for program branches which are two-cycle
- Operating speed: DC - 20 MHz clock input
  DC - 200 ns instruction cycle

Device	Pins	I/O	EPROM/ ROM	RAM
PIC16C54	18	12	512	25
PIC16C54A	18	12	512	25
PIC16C54C	18	12	512	25
PIC16CR54A	18	12	512	25
PIC16CR54C	18	12	512	25
PIC16C55	28	20	512	24
PIC16C55A	28	20	512	24
PIC16C56	18	12	1K	25
PIC16C56A	18	12	1K	25
PIC16CR56A	18	12	1K	25
PIC16C57	28	20	2K	72
PIC16C57C	28	20	2K	72
PIC16CR57C	28	20	2K	72
PIC16C58B	18	12	2K	73
PIC16CR58B	18	12	2K	73

- 12-bit wide instructions
- 8-bit wide data path
- Seven or eight special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

- 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
- Power-on Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable Code Protection
- Power saving SLEEP mode
- Selectable oscillator options:
  - RC: Low-cost RC oscillator
  - XT: Standard crystal/resonator
  - HS: High-speed crystal/resonator
  - LP: Power saving, low-frequency crystal

CMOS Technology:

- Low-power, high-speed CMOS EPROM/ROM technology
- Fully static design
- Wide-operating voltage and temperature range:
  - EPROM Commercial/Industrial 2.0V to 6.25V
  - ROM Commercial/Industrial 2.0V to 6.25V
  - EPROM Extended 2.5V to 6.0V
  - ROM Extended 2.5V to 6.0V
- Low-power consumption
  - < 2 mA typical @ 5V, 4 MHz
  - 15 μA typical @ 3V, 32 kHz
  - < 0.6 μA typical standby current (with WDT disabled) @ 3V, 0°C to 70°C

Note: In this document, figure and table titles refer to all varieties of the part number indicated, (i.e., The title "Figure 14-1: Load Conditions - PIC16C54A", also refers to PIC16LC54A and PIC16LV54A parts) unless specifically called out otherwise.

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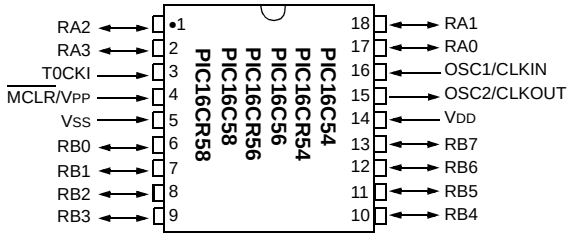
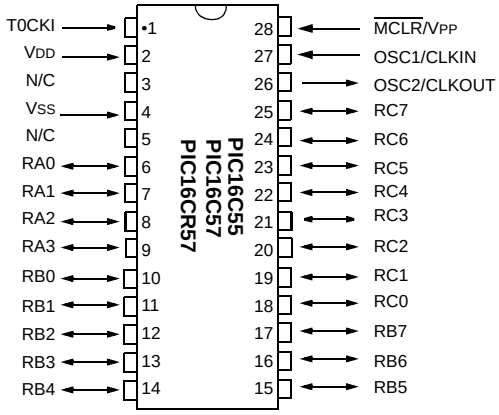
Pin Diagrams

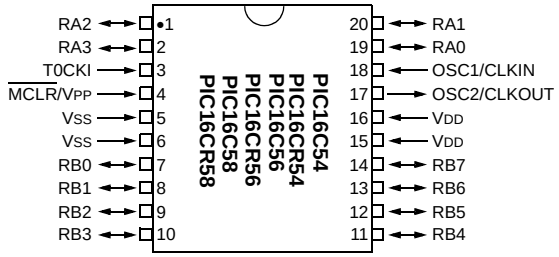
PDIP, SOIC, Windowed CERDIP



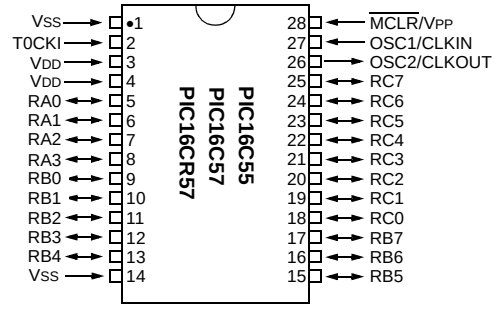
PDIP, SOIC, Windowed CERDIP



SSOP



SSOP



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Device Differences

Device	Voltage Range	Oscillator Selection (Program)	Oscillator	Process Technology (Microns)	ROM Equivalent	$\overline{\text{MCLR}}$ Filter
PIC16C54	2.5-6.25	Factory	See Note 1	1.2	PIC16CR54A	No
PIC16C54A	2.0-6.25	User	See Note 1	0.9	—	No
PIC16C54C	2.5-5.5	User	See Note 1	0.7	PIC16CR54C	Yes
PIC16C55	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C55A	2.5-5.5	User	See Note 1	0.7	—	Yes
PIC16C56	2.5-6.25	Factory	See Note 1	1.7	—	No
PIC16C56A	2.5-5.5	User	See Note 1	0.7	PIC16CR56A	Yes
PIC16C57	2.5-6.25	Factory	See Note 1	1.2	—	No
PIC16C57C	2.5-5.5	User	See Note 1	0.7	PIC16CR57C	Yes
PIC16C58B	2.5-5.5	User	See Note 1	0.7	PIC16CR58B	Yes
PIC16CR54A	2.5-6.25	Factory	See Note 1	1.2	N/A	Yes
PIC16CR54C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR56A	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR57C	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes
PIC16CR58B	2.5-5.5	Factory	See Note 1	0.7	N/A	Yes

Note 1: If you change from this device to another device, please verify oscillator characteristics in your application.

Note: The table shown above shows the generic names of the PIC16C5X devices. For device varieties, please refer to Section 2.0.

Table of Contents

1.0 General Description 5
2.0 PIC16C5X Device Varieties 7
3.0 Architectural Overview 9
4.0 Memory Organization 15
5.0 I/O Ports 25
6.0 Timer0 Module and TMR0 Register 27
7.0 Special Features of the CPU 31
8.0 Instruction Set Summary 43
9.0 Development Support 55
10.0 Electrical Characteristics - PIC16C54/55/56/57 61
11.0 DC and AC Characteristics - PIC16C54/55/56/57 73
12.0 Electrical Characteristics - PIC16CR54A 81
13.0 Electrical Characteristics - PIC16C54A 93
14.0 DC and AC Characteristics - PIC16C54A 105
15.0 Electrical Characteristics - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B 115
16.0 DC and AC Characteristics - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B 127
17.0 Packaging Information 137
Appendix A: Compatibility 149
Index 151
On-Line Support 153
Reader Response 154
PIC16C5X Product Identification System 155
PIC16C54/55/56/57 Product Identification System 156

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1.0 GENERAL DESCRIPTION

The PIC16C5X from Microchip Technology is a family of low-cost, high performance, 8-bit, fully static, EPROM/ROM-based CMOS microcontrollers. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (200 ns) except for program branches which take two cycles. The PIC16C5X delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The PIC16C5X products are equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are four oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and Code Protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost-effective One Time Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers, while benefiting from the OTP's flexibility.

The PIC16C5X products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a low-cost development programmer and a full featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC16C5X series fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices and telecom processors. The EPROM technology makes customizing application programs (transmitter codes, motor speeds, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the PIC16C5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, co-processor applications).

TABLE 1-1: PIC16C5X FAMILY OF DEVICES

		PIC16C54	PIC16CR54	PIC16C55	PIC16C56	PIC16CR56
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20	20
Memory	EPROM Program Memory (x12 words)	512	—	512	1K	—
	ROM Program Memory (x12 words)	—	512	—	—	1K
	RAM Data Memory (bytes)	25	25	24	25	25
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0	TMR0
Features	I/O Pins	12	12	20	12	12
	Number of Instructions	33	33	33	33	33
	Packages	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PICmicro® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.

		PIC16C57	PIC16CR57	PIC16C58	PIC16CR58
Clock	Maximum Frequency of Operation (MHz)	20	20	20	20
Memory	EPROM Program Memory (x12 words)	2K	—	2K	—
	ROM Program Memory (x12 words)	—	2K	—	2K
	RAM Data Memory (bytes)	72	72	73	73
Peripherals	Timer Module(s)	TMR0	TMR0	TMR0	TMR0
Features	I/O Pins	20	20	12	12
	Number of Instructions	33	33	33	33
	Packages	28-pin DIP, SOIC; 28-pin SSOP	28-pin DIP, SOIC; 28-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP	18-pin DIP, SOIC; 20-pin SSOP

All PICmicro® Family devices have Power-on Reset, selectable Watchdog Timer, selectable Code Protect and high I/O current capability.

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2.0 PIC16C5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16C5X Product Identification System at the back of this data sheet to specify the correct part number.

For the PIC16C5X family of devices, there are four device types, as indicated in the device number:

1. **C**, as in PIC16**C**54C. These devices have EPROM program memory and operate over the standard voltage range.
2. **LC**, as in PIC16**LC**54A. These devices have EPROM program memory and operate over an extended voltage range.
3. **CR**, as in PIC16**CR**54A. These devices have ROM program memory and operate over the standard voltage range.
4. **LCR**, as in PIC16**LCR**54A. These devices have ROM program memory and operate over an extended voltage range.

2.1 UV Erasable Devices (EPROM)

The UV erasable versions, offered in CERDIP packages, are optimal for prototype development and pilot programs.

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART® and PRO MATE® programmers both support programming of the PIC16C5X. Third party programmers also are available. Refer to the Third Party Guide for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTP^{SM}) Devices

Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

2.5 Read Only Memory (ROM) Devices

Microchip offers masked ROM versions of several of the highest volume parts, giving the customer a low cost option for high volume, mature products.

NOTES:

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16C5X family can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16C5X uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architecture where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12-bits wide making it possible to have all single word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions (33) execute in a single cycle (200ns @ 20MHz) except for program branches.

The PIC16C54/CR54 and PIC16C55 address 512 x 12 of program memory, the PIC16C56/CR56 address 1K x 12 of program memory, and the PIC16C57/CR57 and PIC16C58/CR58 address 2K x 12 of program memory. All program memory is internal.

The PIC16C5X can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory. The PIC16C5X has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of ‘special optimal situations’ make programming with the PIC16C5X simple yet efficient. In addition, the learning curve is reduced significantly.

The PIC16C5X device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature. In two-operand instructions, typically one operand is the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBWF and ADDWF instructions for examples.

A simplified block diagram is shown in Figure 3-1, with the corresponding device pins described in Table 3-1.

FIGURE 3-1: PIC16C5X SERIES BLOCK DIAGRAM

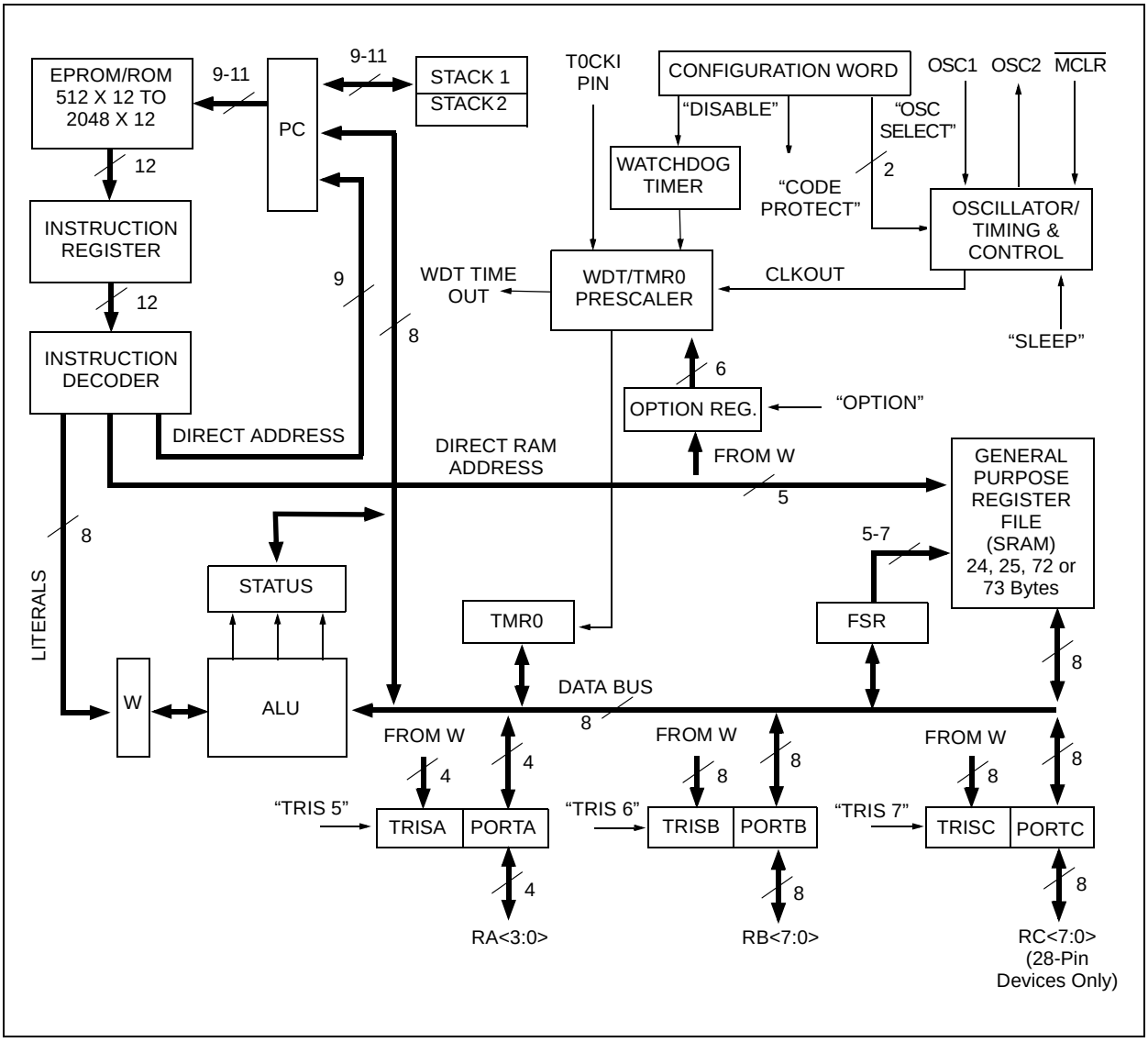

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TABLE 3-1: PINOUT DESCRIPTION - PIC16C54s, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58, PIC16CR58

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	20	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RB0	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	
RB5	11	12	I/O	TTL	
RB6	12	13	I/O	TTL	
RB7	13	14	I/O	TTL	
T0CKI	3	3	I	ST	Clock input to Timer0. Must be tied to V_{SS} or V_{DD}, if not in use, to reduce current consumption.
$\overline{MCLR}/V_{PP}$	4	4	I	ST	Master clear (RESET) input/programming voltage input. This pin is an active low RESET to the device. Voltage on the $\overline{MCLR}/V_{PP}$ pin must not exceed V_{DD} to avoid unintended entering of programming mode.
OSC1/CLKIN	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
V_{DD}	14	15,16	P	—	Positive supply for logic and I/O pins.
V_{SS}	5	5,6	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

TABLE 3-2: PINOUT DESCRIPTION - PIC16C55, PIC16C57, PIC16CR57

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0	6	5	I/O	TTL	Bi-directional I/O port
RA1	7	6	I/O	TTL	
RA2	8	7	I/O	TTL	
RA3	9	8	I/O	TTL	
RB0	10	9	I/O	TTL	Bi-directional I/O port
RB1	11	10	I/O	TTL	
RB2	12	11	I/O	TTL	
RB3	13	12	I/O	TTL	
RB4	14	13	I/O	TTL	
RB5	15	15	I/O	TTL	
RB6	16	16	I/O	TTL	
RB7	17	17	I/O	TTL	
RC0	18	18	I/O	TTL	Bi-directional I/O port
RC1	19	19	I/O	TTL	
RC2	20	20	I/O	TTL	
RC3	21	21	I/O	TTL	
RC4	22	22	I/O	TTL	
RC5	23	23	I/O	TTL	
RC6	24	24	I/O	TTL	
RC7	25	25	I/O	TTL	
T0CKI	1	2	I	ST	Clock input to Timer0. Must be tied to V_{SS} or V_{DD} if not in use to reduce current consumption.
$\overline{MCLR}$	28	28	I	ST	Master clear (RESET) input. This pin is an active low RESET to the device.
OSC1/CLKIN	27	27	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	26	26	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
V_{DD}	2	3,4	P	—	Positive supply for logic and I/O pins.
V_{SS}	4	1,14	P	—	Ground reference for logic and I/O pins.
N/C	3,5	—	—	—	Unused, do not connect.

Legend: I = input, O = output, I/O = input/output, P = power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input

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3.1 Clocking Scheme/Instruction Cycle

The clock input (OSC1/CLKIN pin) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter is incremented every Q1 and the instruction is fetched from program memory and latched into the instruction register in Q4. It is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 3-2 and Example 3-1.

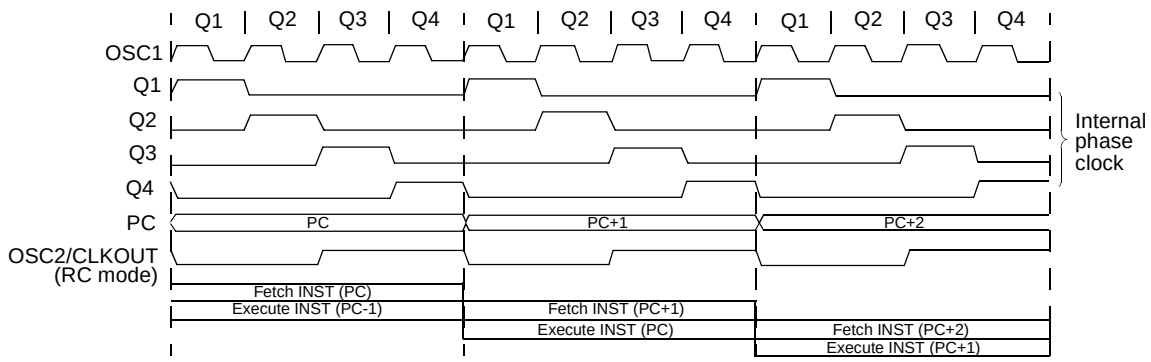
3.2 Instruction Flow/Pipelining

An Instruction Cycle consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 3-1).

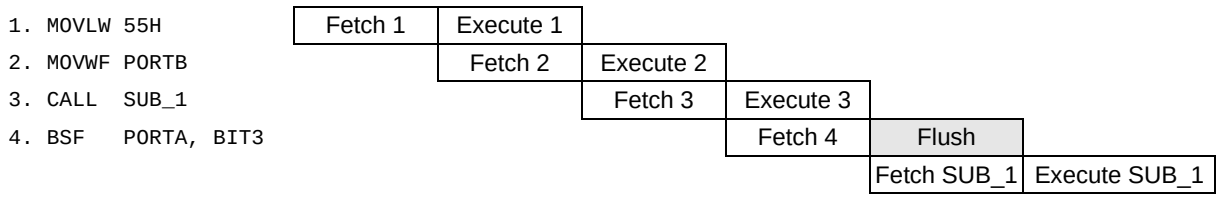
A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

FIGURE 3-2: CLOCK/INSTRUCTION CYCLE



EXAMPLE 3-1: INSTRUCTION PIPELINE FLOW



All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline, while the new instruction is being fetched and then executed.

NOTES:

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4.0 MEMORY ORGANIZATION

PIC16C5X memory is organized into program memory and data memory. For devices with more than 512 bytes of program memory, a paging scheme is used. Program memory pages are accessed using one or two STATUS Register bits. For devices with a data memory register file of more than 32 registers, a banking scheme is used. Data memory banks are accessed using the File Selection Register (FSR).

4.1 Program Memory Organization

The PIC16C54, PIC16CR54 and PIC16C55 have a 9-bit Program Counter (PC) capable of addressing a 512 x 12 program memory space (Figure 4-1). The PIC16C56 and PIC16CR56 have a 10-bit Program Counter (PC) capable of addressing a 1K x 12 program memory space (Figure 4-2). The PIC16CR57, PIC16C58 and PIC16CR58 have an 11-bit Program Counter capable of addressing a 2K x 12 program memory space (Figure 4-3). Accessing a location above the physically implemented address will cause a wraparound.

A NOP at the RESET vector location will cause a restart at location 000h. The RESET vector for the PIC16C54, PIC16CR54 and PIC16C55 is at 1FFh. The RESET vector for the PIC16C56 and PIC16CR56 is at 3FFh. The RESET vector for the PIC16C57, PIC16CR57, PIC16C58, and PIC16CR58 is at 7FFh.

FIGURE 4-1: PIC16C54/CR54/C55 PROGRAM MEMORY MAP AND STACK

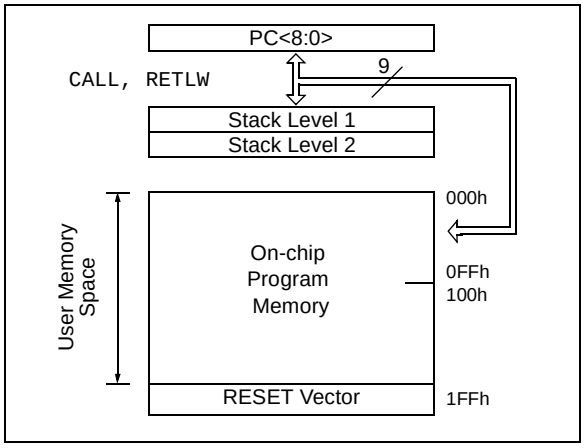


FIGURE 4-2: PIC16C56/CR56 PROGRAM MEMORY MAP AND STACK

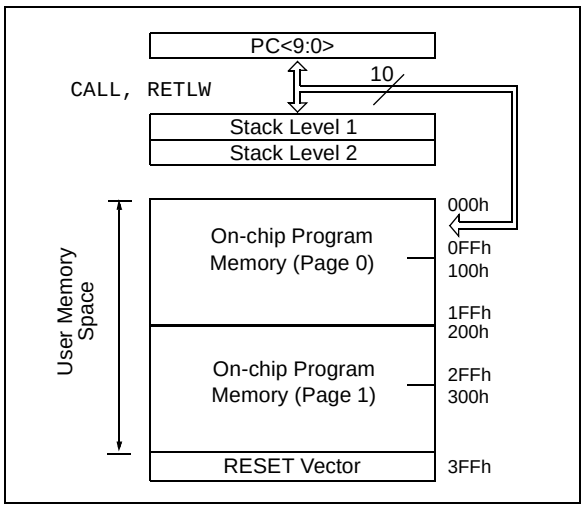
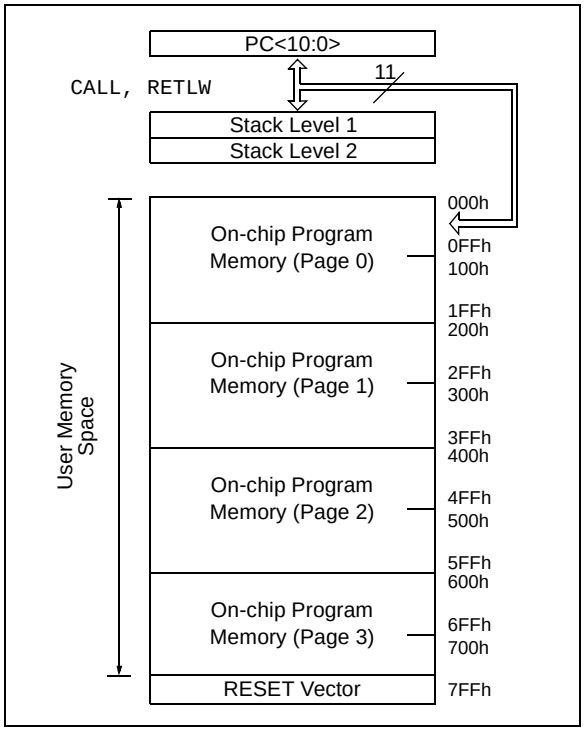


FIGURE 4-3: PIC16C57/CR57/C58/ CR58 PROGRAM MEMORY MAP AND STACK



4.2 Data Memory Organization

Data memory is composed of registers, or bytes of RAM. Therefore, data memory for a device is specified by its register file. The register file is divided into two functional groups: Special Function Registers and General Purpose Registers.

The Special Function Registers include the TMR0 register, the Program Counter (PC), the Status Register, the I/O registers (ports) and the File Select Register (FSR). In addition, Special Purpose Registers are used to control the I/O port configuration and prescaler options.

The General Purpose Registers are used for data and control information under command of the instructions.

For the PIC16C54, PIC16CR54, PIC16C56 and PIC16CR56, the register file is composed of 7 Special Function Registers and 25 General Purpose Registers (Figure 4-4).

For the PIC16C55, the register file is composed of 8 Special Function Registers and 24 General Purpose Registers.

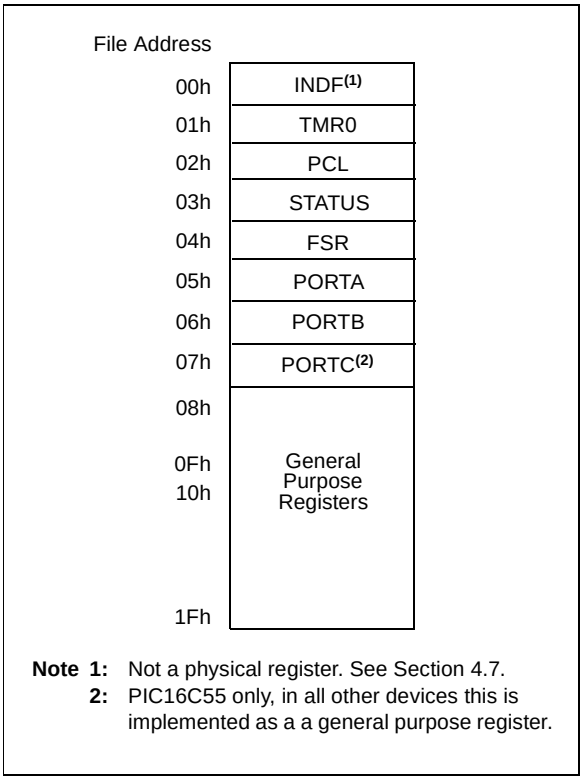
For the PIC16C57 and PIC16CR57, the register file is composed of 8 Special Function Registers, 24 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 4-5).

For the PIC16C58 and PIC16CR58, the register file is composed of 7 Special Function Registers, 25 General Purpose Registers and up to 48 additional General Purpose Registers that may be addressed using a banking scheme (Figure 4-6).

4.2.1 GENERAL PURPOSE REGISTER FILE

The register file is accessed either directly or indirectly through the File Select Register (FSR). The FSR Register is described in Section 4.7.

FIGURE 4-4: PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56 REGISTER FILE MAP



Note 1: Not a physical register. See Section 4.7.
2: PIC16C55 only, in all other devices this is implemented as a a general purpose register.

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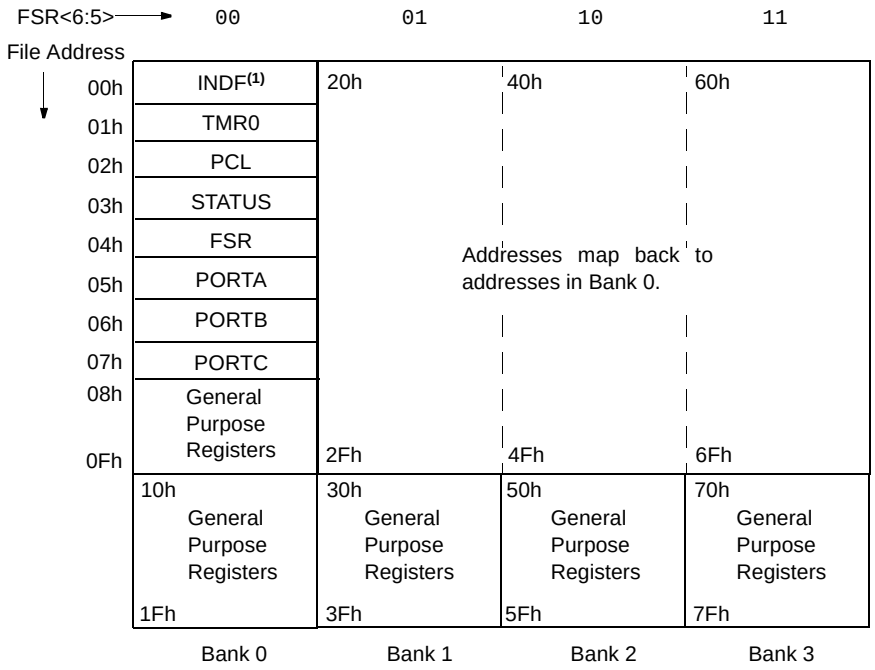
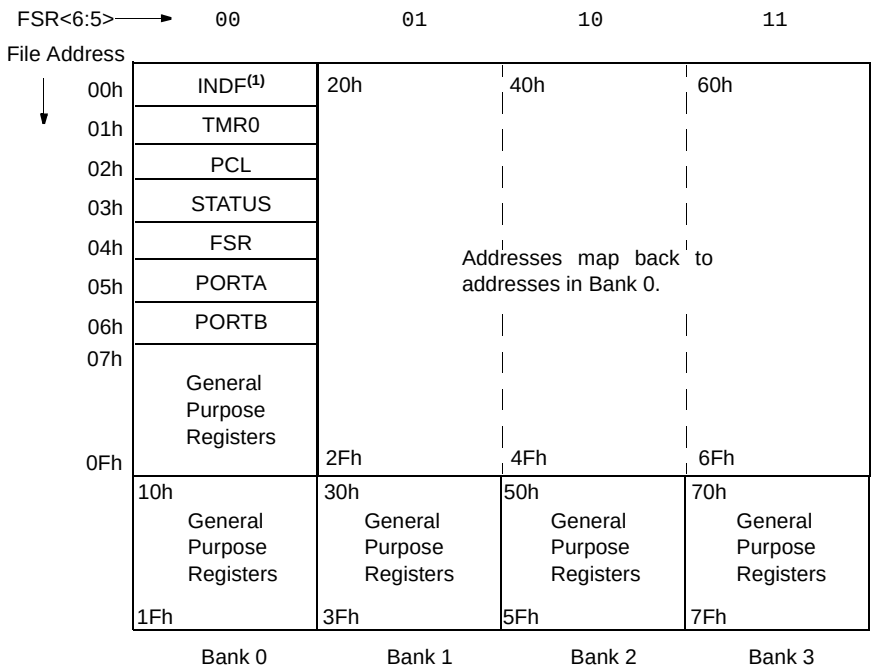
FIGURE 4-5: PIC16C57/CR57 REGISTER FILE MAP



Note 1: Not a physical register. See Section 4.7.

FIGURE 4-6: PIC16C58/CR58 REGISTER FILE MAP



Note 1: Not a physical register. See Section 4.7.

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4.2.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device (Table 4-1).

The Special Registers can be classified into two sets. The Special Function Registers associated with the "core" functions are described in this section. Those related to the operation of the peripheral features are described in the section for each peripheral feature.

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	--11 1111
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h(1)	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								1xxx xxxx(3)	1uuu uuuu(3)
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h(2)	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented or unused, – = unimplemented, read as '0' (if applicable)
x = unknown, u = unchanged, q = see the tables in Section 7.7 for possible values.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.5 for an explanation of how to access these bits.

2: File address 07h is a General Purpose Register on the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58 and PIC16CR58.

3: For the PIC16C54 and PIC16C55, the value on RESET is 111x xxxx and for $\overline{MCLR}$ and WDT Reset, the value is 111u uuuu.

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4.3 STATUS Register

This register contains the arithmetic status of the ALU, the RESET status, and the page preselect bits for program memories larger than 512 words.

The STATUS Register can be the destination for any instruction, as with any other register. If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF and MOVWF instructions be used to alter the STATUS Register because these instructions do not affect the Z, DC or C bits from the STATUS Register. For other instructions which do affect STATUS Bits, see Section 8.0, Instruction Set Summary.

REGISTER 4-1: STATUS REGISTER (ADDRESS:03h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
PA2	PA1	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit7	6	5	4	3	2	1	bit0

R = Readable bit
W = Writable bit
- n = Value at POR reset

bit 7: **PA2**: This bit unused at this time.
Use of the PA2 bit as a general purpose read/write bit is not recommended, since this may affect upward compatibility with future products.

bit 6-5: **PA<1:0>**: Program page preselect bits (PIC16C56/CR56)(PIC16C57/CR57)(PIC16C58/CR58)
00 = Page 0 (000h - 1FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58
01 = Page 1 (200h - 3FFh) - PIC16C56/CR56, PIC16C57/CR57, PIC16C58/CR58
10 = Page 2 (400h - 5FFh) - PIC16C57/CR57, PIC16C58/CR58
11 = Page 3 (600h - 7FFh) - PIC16C57/CR57, PIC16C58/CR58
Each page is 512 words.
Using the PA<1:0> bits as general purpose read/write bits in devices which do not use them for program page preselect is not recommended since this may affect upward compatibility with future products.

bit 4: **$\overline{TO}$**: Time-out bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred

bit 3: **$\overline{PD}$**: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2: **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1: **DC**: Digit carry/$\overline{borrow}$ bit (for ADDWF and SUBWF instructions)
ADDWF
1 = A carry from the 4th low order bit of the result occurred
0 = A carry from the 4th low order bit of the result did not occur
SUBWF
1 = A borrow from the 4th low order bit of the result did not occur
0 = A borrow from the 4th low order bit of the result occurred

bit 0: **C**: Carry/$\overline{borrow}$ bit (for ADDWF, SUBWF and RRF, RLF instructions)

ADDWF	SUBWF	RRF or RLF
1 = A carry occurred	1 = A borrow did not occur	Loaded with LSb or MSb, respectively
0 = A carry did not occur	0 = A borrow occurred	

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4.4 OPTION Register

The OPTION Register is a 6-bit wide, write-only register which contains various control bits to configure the Timer0/WDT prescaler and Timer0.

By executing the `OPTION` instruction, the contents of the W Register will be transferred to the OPTION Register. A RESET sets the OPTION<5:0> bits.

REGISTER 4-2: OPTION REGISTER

U-0	U-0	W-1	W-1	W-1	W-1	W-1	W-1
—	—	T0CS	T0SE	PSA	PS2	PS1	PS0
bit7	6	5	4	3	2	1	bit0

W = Writable bit
U = Unimplemented bit
- n = Value at POR reset

bit 7-6: **Unimplemented**.

bit 5: **T0CS**: Timer0 clock source select bit
`1` = Transition on T0CKI pin
`0` = Internal instruction cycle clock (CLKOUT)

bit 4: **T0SE**: Timer0 source edge select bit
`1` = Increment on high-to-low transition on T0CKI pin
`0` = Increment on low-to-high transition on T0CKI pin

bit 3: **PSA**: Prescaler assignment bit
`1` = Prescaler assigned to the WDT
`0` = Prescaler assigned to Timer0

bit 2-0: **PS<2:0>**: Prescaler rate select bits

Bit Value	Timer0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

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4.5 Program Counter

As a program instruction is executed, the Program Counter (PC) will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, bits 8:0 of the PC are provided by the GOTO instruction word. The PC Latch (PCL) is mapped to PC<7:0> (Figure 4-7 and Figure 4-8).

For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number must be supplied as well. Bit5 and bit6 of the STATUS Register provide page information to bit9 and bit10 of the PC (Figure 4-8 and Figure 4-9).

For a CALL instruction, or any instruction where the PCL is the destination, bits 7:0 of the PC again are provided by the instruction word. However, PC<8> does not come from the instruction word, but is always cleared (Figure 4-7 and Figure 4-8).

Instructions where the PCL is the destination, or Modify PCL instructions, include MOVWF PC, ADDWF PC, and BSF PC,5.

For the PIC16C56, PIC16CR56, PIC16C57, PIC16CR57, PIC16C58 and PIC16CR58, a page number again must be supplied. Bit5 and bit6 of the STATUS Register provide page information to bit9 and bit10 of the PC (Figure 4-8 and Figure 4-9).

Note:	Because PC<8> is cleared in the CALL instruction, or any Modify PCL instruction, all subroutine calls or computed jumps are limited to the first 256 locations of any program memory page (512 words long).

FIGURE 4-7: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C54, PIC16CR54, PIC16C55

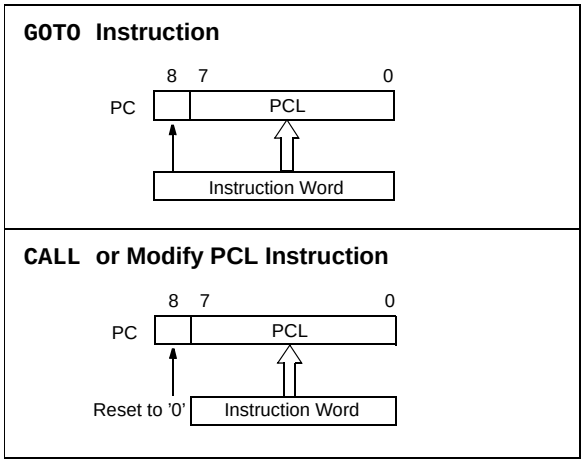


FIGURE 4-8: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C56/PIC16CR56

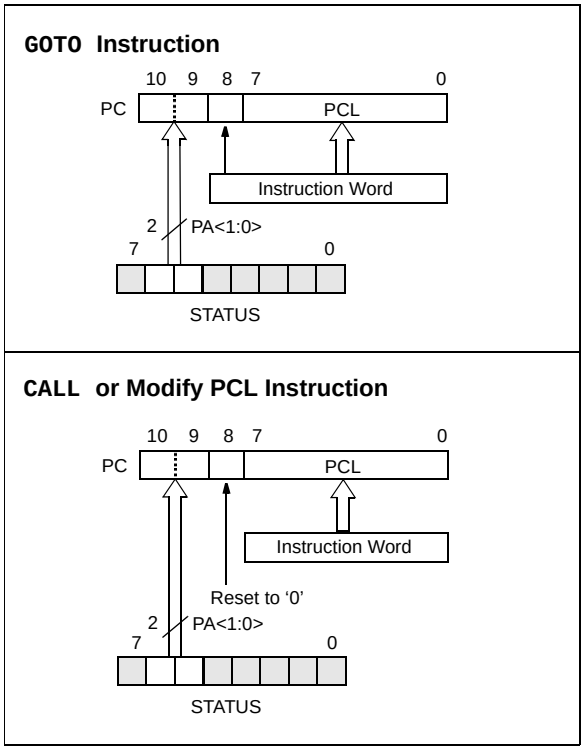
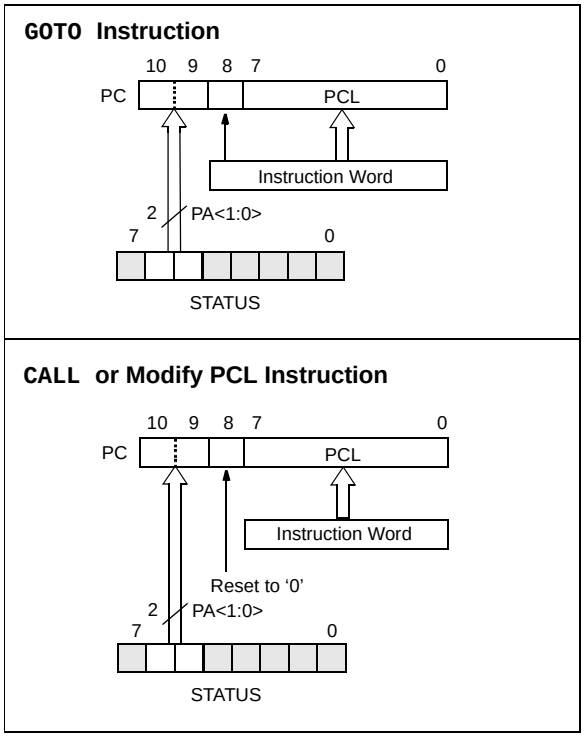


FIGURE 4-9: LOADING OF PC BRANCH INSTRUCTIONS - PIC16C57/PIC16CR57, AND PIC16C58/PIC16CR58



4.5.1 PAGING CONSIDERATIONS – PIC16C56/CR56, PIC16C57/CR57 AND PIC16C58/CR58

If the Program Counter is pointing to the last address of a selected memory page, when it increments it will cause the program to continue in the next higher page. However, the page preselect bits in the STATUS Register will not be updated. Therefore, the next GOTO, CALL or modify PCL instruction will send the program to the page specified by the page preselect bits (PA0 or PA<1:0>).

For example, a NOP at location 1FFh (page 0) increments the PC to 200h (page 1). A GOTO xxx at 200h will return the program to address 0xxh on page 0 (assuming that PA<1:0> are clear).

To prevent this, the page preselect bits must be updated under program control.

4.5.2 EFFECTS OF RESET

The Program Counter is set upon a RESET, which means that the PC addresses the last location in the last page (e.g., the RESET vector).

The STATUS Register page preselect bits are cleared upon a RESET, which means that page 0 is pre-selected.

Therefore, upon a RESET, a GOTO instruction at the RESET vector location will automatically cause the program to jump to page 0.

4.6 Stack

PIC16C5X devices have a 10-bit or 11-bit wide, two-level hardware push/pop stack.

A CALL instruction will push the current value of stack 1 into stack 2 and then push the current program counter value, incremented by one, into stack level 1. If more than two sequential CALL's are executed, only the most recent two return addresses are stored.

A RETLW instruction will pop the contents of stack level 1 into the program counter and then copy stack level 2 contents into level 1. If more than two sequential RETLW's are executed, the stack will be filled with the address previously stored in level 2. Note that the W Register will be loaded with the literal value specified in the instruction. This is particularly useful for the implementation of data look-up tables within the program memory.

For the RETLW instruction, the PC is loaded with the Top of Stack (TOS) contents. All of the devices covered in this data sheet have a two-level stack. The stack has the same bit width as the device PC.

4.7 Indirect Data Addressing; INDF and FSR Registers

The INDF Register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR Register (FSR is a *pointer*). This is indirect addressing.

EXAMPLE 4-1: INDIRECT ADDRESSING

- Register file 08 contains the value 10h
- Register file 09 contains the value 0Ah
- Load the value 08 into the FSR Register
- A read of the INDF Register will return the value of 10h
- Increment the value of the FSR Register by one (FSR = 09h)
- A read of the INDR register now will return the value of 0Ah.

Reading INDF itself indirectly (FSR = 0) will produce 00h. Writing to the INDF Register indirectly results in a no-operation (although STATUS bits may be affected).

A simple program to clear RAM locations 10h-1Fh using indirect addressing is shown in Example 4-2.

EXAMPLE 4-2: HOW TO CLEAR RAM USING INDIRECT ADDRESSING

```
            movlw   0x10    ;initialize pointer
            movwf   FSR     ; to RAM
NEXT        clrf    INDF    ;clear INDF Register
            incf    FSR,F   ;inc pointer
            btfsc   FSR,4   ;all done?
            goto    NEXT    ;NO, clear next
CONTINUE
            :               ;YES, continue
```

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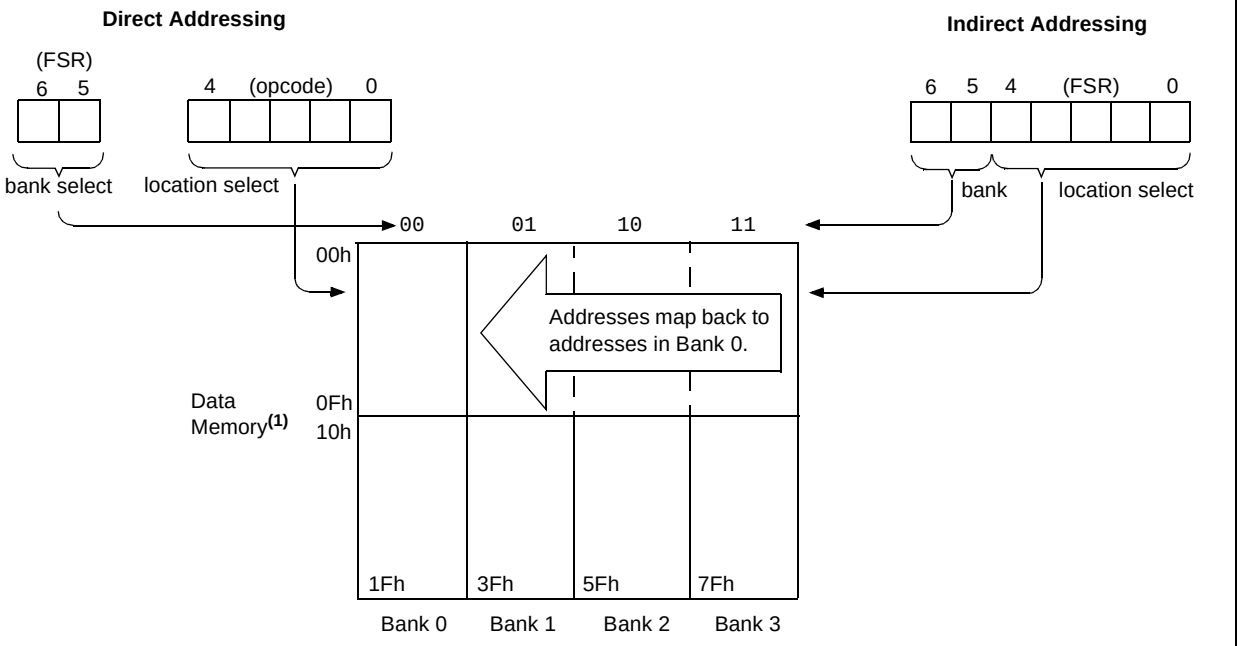
The FSR is either a 5-bit (PIC16C54, PIC16CR54, PIC16C55), 6-bit (PIC16C56, PIC16CR56), or 7-bit (PIC16C57s, PIC16CR57, PIC16C58, PIC16CR58) wide register. It is used in conjunction with the INDF Register to indirectly address the data memory area.

The FSR<4:0> bits are used to select data memory addresses 00h to 1Fh.

PIC16C54, PIC16CR54, PIC16C55: These do not use banking. FSR<6:5> bits are unimplemented and read as '1's.

PIC16C57, PIC16CR57, PIC16C58, PIC16CR58: FSR<6:5> are the bank select bits and are used to select the bank to be addressed (00 = bank 0, 01 = bank 1, 10 = bank 2, 11 = bank 3).

FIGURE 4-10: DIRECT/INDIRECT ADDRESSING



Note 1: For register map detail see Section 4.2.

NOTES:

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5.0 I/O PORTS

As with any other register, the I/O Registers can be written and read under program control. However, read instructions (e.g., MOVF PORTB,W) always read the I/O pins independent of the pin's input/output modes. On RESET, all I/O ports are defined as input (inputs are at hi-impedance) since the I/O control registers (TRISA, TRISB, TRISC) are all set.

5.1 PORTA

PORTA is a 4-bit I/O Register. Only the low order 4 bits are used (RA<3:0>). Bits 7-4 are unimplemented and read as '0's.

5.2 PORTB

PORTB is an 8-bit I/O Register (PORTB<7:0>).

5.3 PORTC

PORTC is an 8-bit I/O Register for PIC16C55, PIC16C57 and PIC16CR57.

PORTC is a General Purpose Register for PIC16C54, PIC16CR54, PIC16C56, PIC16C58 and PIC16CR58.

5.4 TRIS Registers

The Output Driver Control Registers are loaded with the contents of the W Register by executing the TRIS f instruction. A '1' from a TRIS Register bit puts the corresponding output driver in a hi-impedance (input) mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer.

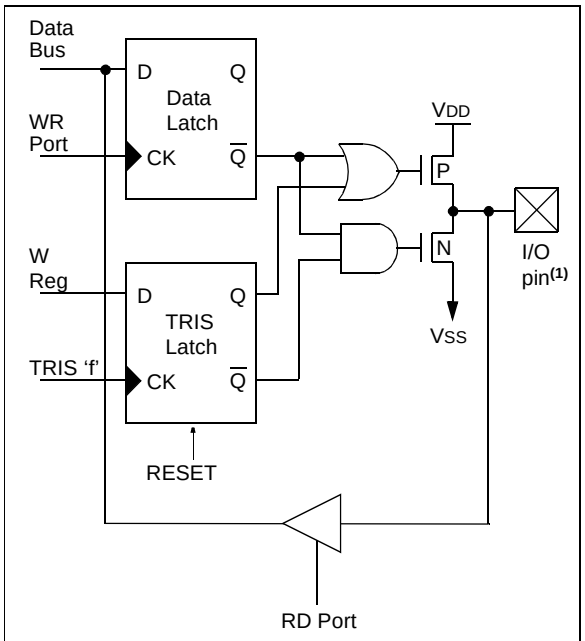
Note:	A read of the ports reads the pins, not the output data latches. That is, if an output driver on a pin is enabled and driven high, but the external system is holding it low, a read of the port will indicate that the pin is low.

The TRIS Registers are "write-only" and are set (output drivers disabled) upon RESET.

5.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 5-1. All ports may be used for both input and output operation. For input operations these ports are non-latching. Any input must be present until read by an input instruction (e.g., MOVF PORTB, W). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit (in TRISA, TRISB) must be cleared (= 0). For use as an input, the corresponding TRIS bit must be set. Any I/O pin can be programmed individually as input or output.

FIGURE 5-1: EQUIVALENT CIRCUIT FOR A SINGLE I/O PIN



Note 1: I/O pins have protection diodes to VDD and VSS.

TABLE 5-1: SUMMARY OF PORT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
07h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented, read as '0', — = unimplemented, read as '0', x = unknown, u = unchanged

5.6 I/O Programming Considerations

5.6.1 BI-DIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and re-write the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (say bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Example 5-1 shows the effect of two sequential read-modify-write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired-or", "wired-and"). The resulting high output currents may damage the chip.

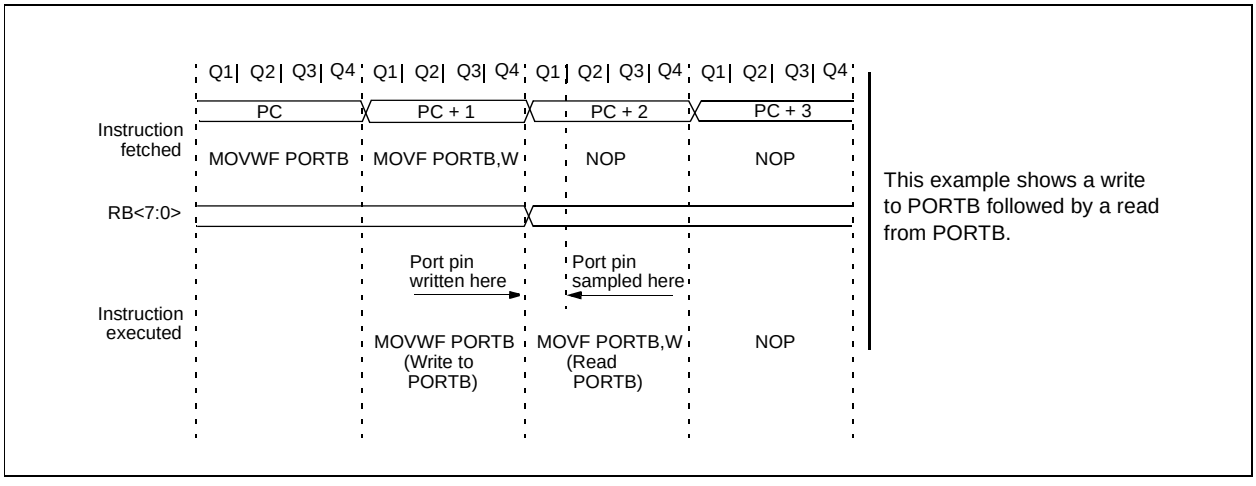
EXAMPLE 5-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
;Initial PORT Settings
; PORTB<7:4> Inputs
; PORTB<3:0> Outputs
;PORTB<7:6> have external pull-ups and are
;not connected to other circuitry
;
;                   PORT latch  PORT pins
;                   ----------  ----------
  BCF   PORTB, 7   ;01pp pppp   11pp pppp
  BCF   PORTB, 6   ;10pp pppp   11pp pppp
  MOVLW 03Fh       ;
  TRIS  PORTB      ;10pp pppp   10pp pppp
;
;Note that the user may have expected the pin
;values to be 00pp pppp. The 2nd BCF caused
;RB7 to be latched as the pin value (High).
```

5.6.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 5-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction, which causes that file to be read into the CPU, is executed. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

FIGURE 5-2: SUCCESSIVE I/O OPERATION



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6.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
  - Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
  - Edge select for external clock

Figure 6-1 is a simplified block diagram of the Timer0 module, while Figure 6-2 shows the electrical structure of the Timer0 input.

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (Figure 6-3 and Figure 6-4). The user can work around this by writing an adjusted value to the TMR0 register.

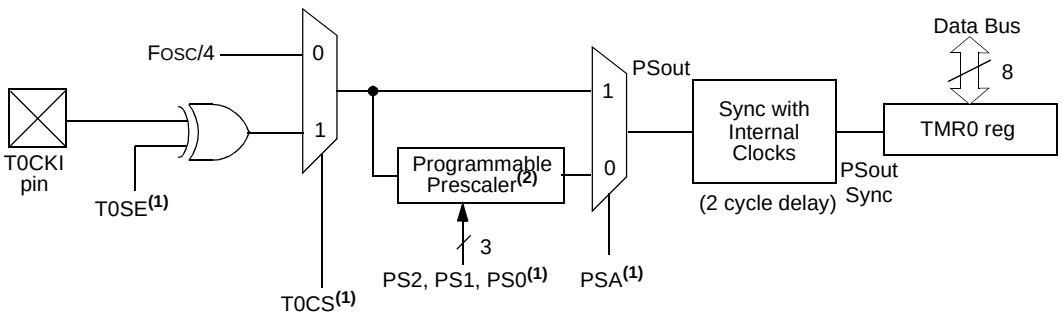
Counter mode is selected by setting the T0CS bit (OPTION<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in Section 6.1.

Note:	The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both.

The prescaler assignment is controlled in software by the control bit PSA (OPTION<3>). Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. Section 6.2 details the operation of the prescaler.

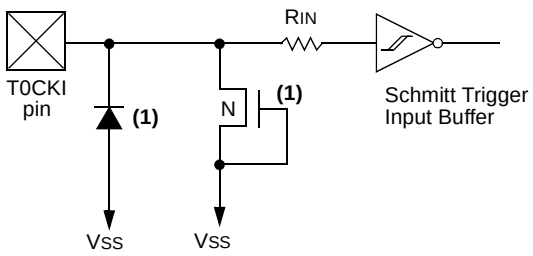
A summary of registers associated with the Timer0 module is found in Table 6-1.

FIGURE 6-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register.
2: The prescaler is shared with the Watchdog Timer (Figure 6-6).

FIGURE 6-2: ELECTRICAL STRUCTURE OF T0CKI PIN



Note 1: ESD protection circuits.

FIGURE 6-3: TIMER0 TIMING: INTERNAL CLOCK/NO PRESCALE

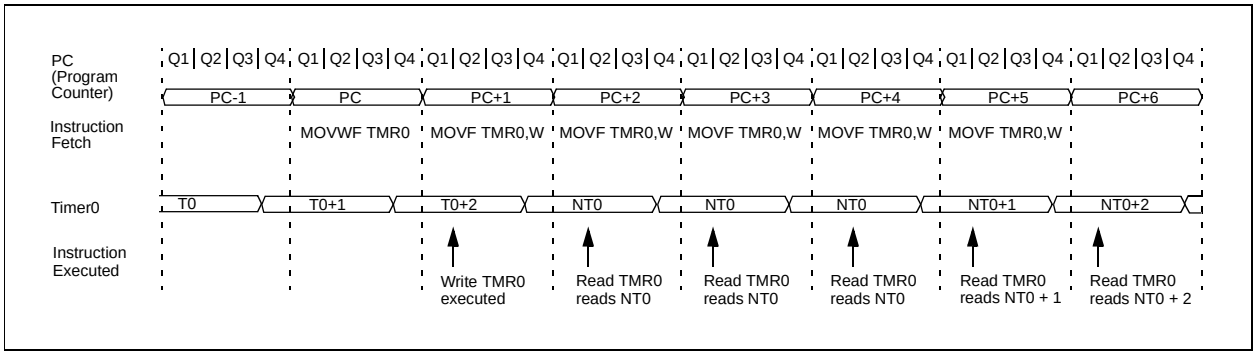


FIGURE 6-4: TIMER0 TIMING: INTERNAL CLOCK/PRESCALE 1:2

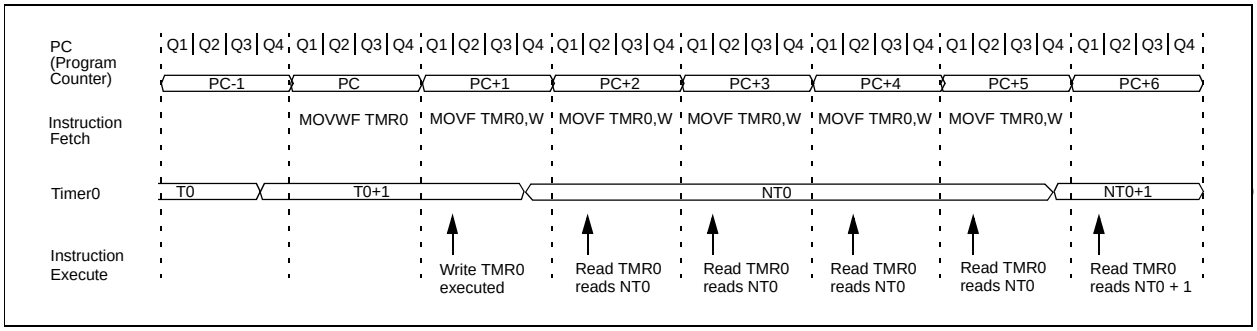


TABLE 6-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on MCLR and WDT Reset
01h	TMR0	Timer0 - 8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: Shaded cells: Unimplemented bits, - = unimplemented, x = unknown, u = unchanged.

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6.1 Using Timer0 with an External Clock

When an external clock input is used for Timer0, it must meet certain requirements. The external clock requirement is due to internal phase clock (TOSC) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

6.1.1 EXTERNAL CLOCK SYNCHRONIZATION

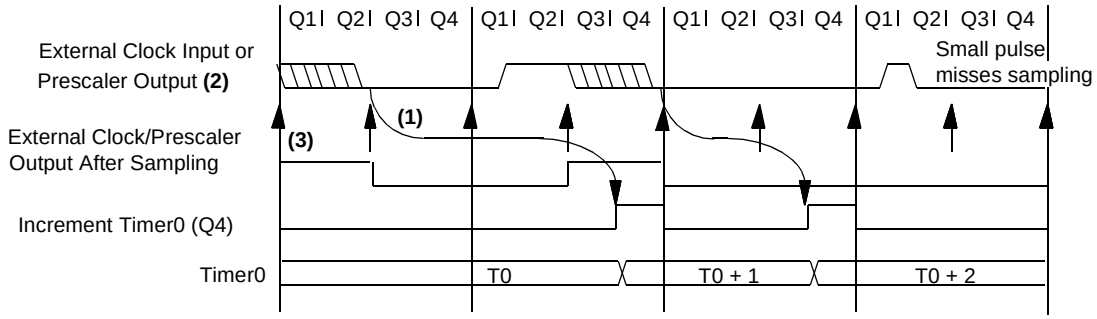
When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks (Figure 6-5). Therefore, it is necessary for T0CKI to be high for at least 2TOSC (and a small RC delay of 20 ns) and low for at least 2TOSC (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

When a prescaler is used, the external clock input is divided by the asynchronous ripple counter-type prescaler so that the prescaler output is symmetrical. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4TOSC (and a small RC delay of 40 ns) divided by the prescaler value. The only requirement on T0CKI high and low time is that they do not violate the minimum pulse width requirement of 10 ns. Refer to parameters 40, 41 and 42 in the electrical specification of the desired device.

6.1.2 TIMER0 INCREMENT DELAY

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time the Timer0 module is actually incremented. Figure 6-5 shows the delay from the external clock edge to the timer incrementing.

FIGURE 6-5: TIMER0 TIMING WITH EXTERNAL CLOCK



Note 1: Delay from clock input change to Timer0 increment is 3Tosc to 7Tosc. (Duration of Q = Tosc). Therefore, the error in measuring the interval between two edges on Timer0 input = ± 4Tosc max.

2: External clock if no prescaler selected, prescaler output otherwise.

3: The arrows indicate the points in time where sampling occurs.

6.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer (WDT), respectively (Section 6.1.2). For simplicity, this counter is being referred to as “prescaler” throughout this data sheet. Note that the prescaler may be used by either the Timer0 module or the WDT, but not both. Thus, a prescaler assignment for the Timer0 module means that there is no prescaler for the WDT, and vice-versa.

The PSA and PS<2:0> bits (OPTION<3:0>) determine prescaler assignment and prescale ratio.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., `CLRF 1`, `MOVWF 1`, `BSF 1,x`, etc.) will clear the prescaler. When assigned to WDT, a `CLRWDT` instruction will clear the prescaler along with the WDT. The prescaler is neither readable nor writable. On a RESET, the prescaler contains all '0's.

6.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed “on the fly” during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 6-1) must be executed when changing the prescaler assignment from Timer0 to the WDT.

EXAMPLE 6-1: CHANGING PRESCALER (TIMER0→WDT)

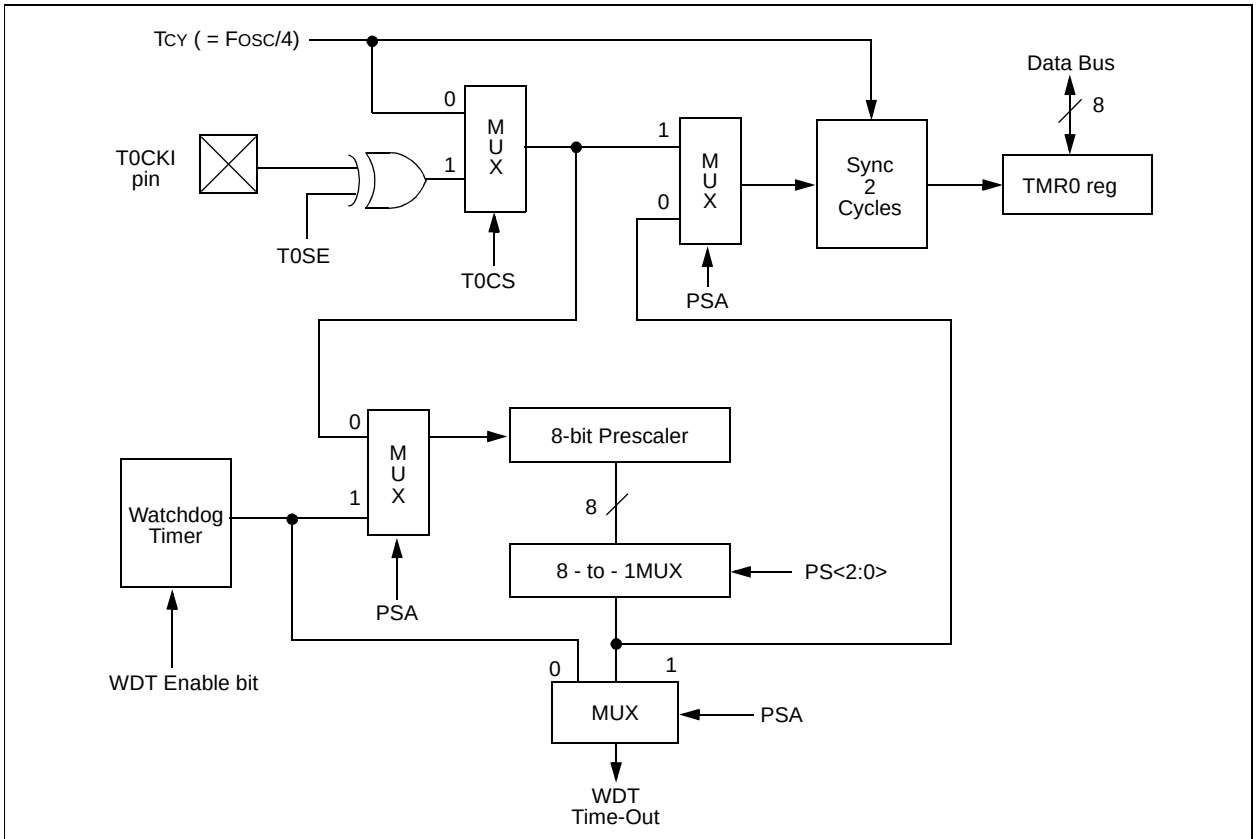
```
1.CLRWDT              ;Clear WDT
2.CLRF   TMR0         ;Clear TMR0 & Prescaler
3.MOVLW  '00xx1111'b  ;These 3 lines (5, 6, 7)
4.OPTION              ; are required only if
                      ; desired
5.CLRWDT              ;PS<2:0> are 000 or
                      ;001
6.MOVLW  '00xx1xxx'b  ;Set Postscaler to
7.OPTION              ; desired WDT rate
```

To change prescaler from the WDT to the Timer0 module, use the sequence shown in Example 6-2. This sequence must be used even if the WDT is disabled. A `CLRWDT` instruction should be executed before switching the prescaler.

EXAMPLE 6-2: CHANGING PRESCALER (WDT→TIMER0)

```
CLRWDT                ;Clear WDT and
                      ;prescaler
MOVLW   'xxxx0xxx'    ;Select TMR0, new
                      ;prescale value and
                      ;clock source
OPTION
```

FIGURE 6-6: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



Note: T0CS, T0SE, PSA, PS<2:0> are bits in the OPTION register.

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7.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16C5X family of microcontrollers has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These features are:

- Oscillator selection
- RESET
- Power-on Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT)
- SLEEP
- Code Protection
- ID locations

The PIC16C5X Family has a Watchdog Timer, which can be shut off only through configuration bit WDTE. It runs off of its own RC oscillator for added reliability. There is an 18 ms delay provided by the Device Reset Timer (DRT), intended to keep the chip in RESET until the crystal oscillator is stable. With this timer on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external RESET or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options.

7.1 Configuration Bits

Configuration bits can be programmed to select various device configurations. Two bits are for the selection of the oscillator type and one bit is the Watchdog Timer enable bit. Nine bits are code protection bits (Figure 7-1 and Figure 7-2) for the PIC16C54, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58, and PIC16CR58 devices.

QTP or ROM devices have the oscillator configuration programmed at the factory and these parts are tested accordingly (see "Product Identification System" diagrams in the back of this data sheet).

FIGURE 7-1: CONFIGURATION WORD FOR PIC16CR54A/C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B

CP	CP	CP	CP	CP	CP	CP	CP	CP	WDTE	FOSC1	FOSC0
bit11	10	9	8	7	6	5	4	3	2	1	bit0

Register: CONFIG
Address(1): FFFh

bit 11-3: **CP:** Code protection bits
1 = Code protection off
0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **Fosc1:Fosc0:** Oscillator selection bits
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Refer to the PIC16C5X Programming Specification (Literature Number DS30190) to determine how to access the configuration word.

FIGURE 7-2: CONFIGURATION WORD FOR PIC16C54/C54A/C55/C56/C57

—	—	—	—	—	—	—	—	CP	WDTE	FOSC1	FOSC0
bit11	10	9	8	7	6	5	4	3	2	1	bit0

Register:	CONFIG
Address(1):	FFFh

bit 11-4: **Unimplemented:** Read as '0'

bit 3: **CP:** Code protection bit.
1 = Code protection off
0 = Code protection on

bit 2: **WDTE:** Watchdog timer enable bit
1 = WDT enabled
0 = WDT disabled

bit 1-0: **Fosc1:Fosc0:** Oscillator selection bits(2)
11 = RC oscillator
10 = HS oscillator
01 = XT oscillator
00 = LP oscillator

Note 1: Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.
2: PIC16LV54A supports XT, RC and LP oscillator only.
PIC16LV58A supports XT, RC and LP oscillator only.

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7.2 Oscillator Configurations

7.2.1 OSCILLATOR TYPES

PIC16C5Xs can be operated in four different oscillator modes. The user can program two configuration bits (FOSC<1:0>) to select one of these four modes:

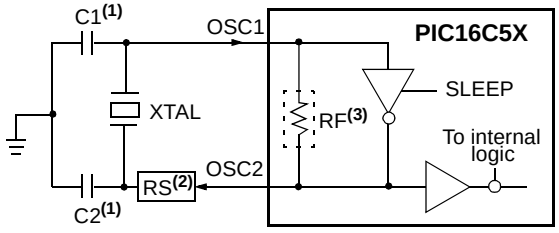
- LP: Low Power Crystal
- XT: Crystal/Resonator
- HS: High Speed Crystal/Resonator
- RC: Resistor/Capacitor

Note:	Not all oscillator selections available for all parts. See Section 7.1.

7.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 7-3). The PIC16C5X oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source drive the OSC1/CLKIN pin (Figure 7-4).

FIGURE 7-3: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)



Note 1: See Capacitor Selection tables for recommended values of C1 and C2.
2: A series resistor (RS) may be required for AT strip cut crystals.
3: RF varies with the crystal chosen (approx. value = 10 MΩ).

FIGURE 7-4: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

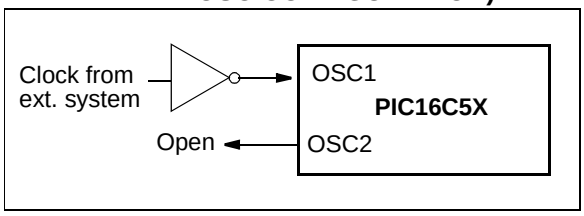


TABLE 7-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS - PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap. Range C1	Cap. Range C2
XT	455 kHz	22-100 pF	22-100 pF
	2.0 MHz	15-68 pF	15-68 pF
	4.0 MHz	15-68 pF	15-68 pF
HS	4.0 MHz	15-68 pF	15-68 pF
	8.0 MHz	10-68 pF	10-68 pF
	16.0 MHz	10-22 pF	10-22 pF

Note: These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 7-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR - PIC16C5X, PIC16CR5X

Osc Type	Resonator Freq	Cap.Range C1	Cap. Range C2
LP	32 kHz(1)	15 pF	15 pF
	100 kHz	15-30 pF	30-47 pF
	200 kHz	15-30 pF	15-82 pF
XT	100 kHz	15-30 pF	200-300 pF
	200 kHz	15-30 pF	100-200 pF
	455 kHz	15-30 pF	15-100 pF
	1 MHz	15-30 pF	15-30 pF
	2 MHz	15-30 pF	15-30 pF
	4 MHz	15-47 pF	15-47 pF
HS	4 MHz	15-30 pF	15-30 pF
	8 MHz	15-30 pF	15-30 pF
	20 MHz	15-30 pF	15-30 pF

Note 1: For VDD > 4.5V, C1 = C2 ≈ 30 pF is recommended.
2: These values are for design guidance only. Rs may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

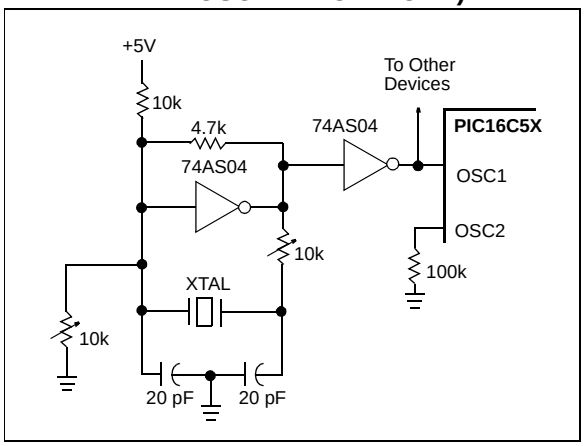
Note:	If you change from one device to another device, please verify oscillator characteristics in your application.

7.2.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance or one with series resonance.

Figure 7-5 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

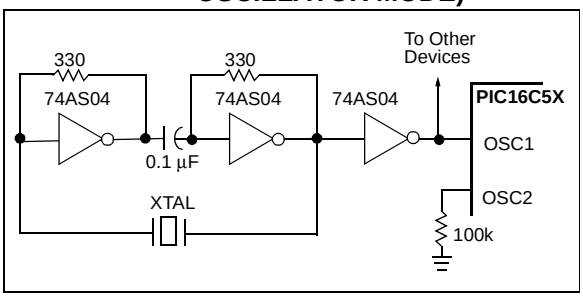
FIGURE 7-5: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)



Note:	If you change from one device to another device, please verify oscillator characteristics in your application.

This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330 Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 7-6: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT (USING XT, HS OR LP OSCILLATOR MODE)



Note:	If you change from one device to another device, please verify oscillator characteristics in your application.

7.2.4 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 7-7 shows how the R/C combination is connected to the PIC16C5X. For REXT values below 2.2 kΩ, the oscillator operation may become unstable, or stop completely. For very high REXT values (e.g., 1 MΩ) the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping REXT between 3 kΩ and 100 kΩ.

Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With no or small external capacitance, the oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

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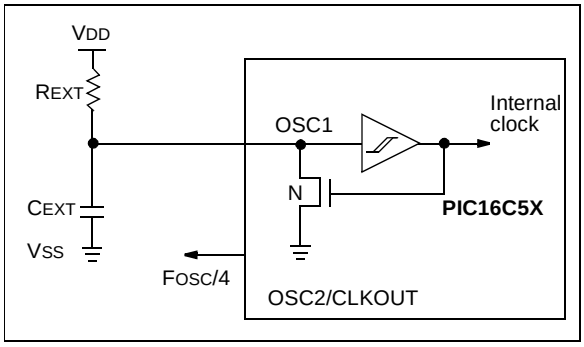
The Electrical Specification sections show RC frequency variation from part to part due to normal process variation.

Also, see the Electrical Specification sections for variation of oscillator frequency due to VDD for given REXT/CEXT values, as well as frequency variation due to operating temperature for given R, C and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin, and can be used for test purposes or to synchronize other logic.

FIGURE 7-7: RC OSCILLATOR MODE



Note:	If you change from one device to another device, please verify oscillator characteristics in your application.

7.3 RESET

PIC16C5X devices may be RESET in one of the following ways:

- Power-on Reset (POR)
- $\overline{\text{MCLR}}$ Reset (normal operation)
- $\overline{\text{MCLR}}$ Wake-up Reset (from SLEEP)
- WDT Reset (normal operation)
- WDT Wake-up Reset (from SLEEP)

Table 7-3 shows these RESET conditions for the PCL and STATUS registers.

Some registers are not affected in any RESET condition. Their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a "RESET state" on Power-on Reset (POR), $\overline{\text{MCLR}}$ or WDT Reset. A $\overline{\text{MCLR}}$ or WDT Wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits (STATUS <4:3>) are set or cleared depending on the different RESET conditions (Section 7.7). These bits may be used to determine the nature of the RESET.

Table 7-4 lists a full description of RESET states of all registers. Figure 7-8 shows a simplified block diagram of the on-chip RESET circuit.

TABLE 7-3: RESET CONDITIONS FOR SPECIAL REGISTERS

Condition	PCL Addr: 02h	STATUS Addr: 03h
Power-on Reset	1111 1111	0001 1xxx
$\overline{MCLR}$ Reset (normal operation)	1111 1111	000u uuuu(1)
$\overline{MCLR}$ Wake-up (from SLEEP)	1111 1111	0001 0uuu
WDT Reset (normal operation)	1111 1111	0000 uuuu(2)
WDT Wake-up (from SLEEP)	1111 1111	0000 0uuu

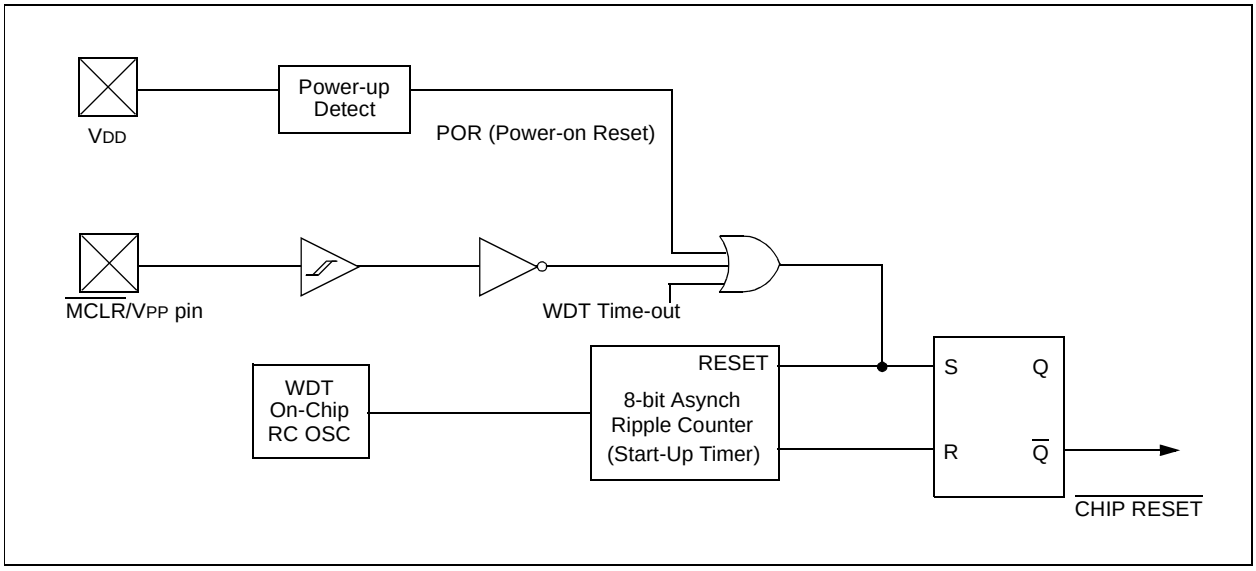
Legend: u = unchanged, x = unknown, - = unimplemented read as '0'.
Note 1: $\overline{TO}$ and $\overline{PD}$ bits retain their last value until one of the other RESET conditions occur.
2: The CLRWDT instruction will set the $\overline{TO}$ and $\overline{PD}$ bits.

TABLE 7-4: RESET CONDITIONS FOR ALL REGISTERS

Register	Address	Power-on Reset	$\overline{MCLR}$ or WDT Reset
W	N/A	xxxx xxxx	uuuu uuuu
TRIS	N/A	1111 1111	1111 1111
OPTION	N/A	--11 1111	--11 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL(1)	02h	1111 1111	1111 1111
STATUS(1)	03h	0001 1xxx	000q quuu
FSR	04h	1xxx xxxx	1uuu uuuu
PORTA	05h	---- xxxx	---- uuuu
PORTB	06h	xxxx xxxx	uuuu uuuu
PORTC(2)	07h	xxxx xxxx	uuuu uuuu
General Purpose Register Files	07-7Fh	xxxx xxxx	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, read as '0',
q = see tables in Section 7.7 for possible values.
Note 1: See Table 7-3 for RESET value for specific conditions.
2: General purpose register file on PIC16C54/CR54/C56/CR56/C58/CR58.

FIGURE 7-8: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



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7.4 Power-on Reset (POR)

The PIC16C5X family incorporates on-chip Power-on Reset (POR) circuitry which provides an internal chip RESET for most power-up situations. To use this feature, the user merely ties the MCLR/VPP pin to VDD. A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 7-8.

The Power-on Reset circuit and the Device Reset Timer (Section 7.5) circuit are closely related. On power-up, the Reset Latch is set and the DRT is RESET. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, which is typically 18 ms, it will reset the Reset Latch and thus end the on-chip RESET signal.

A power-up example where MCLR is not tied to VDD is shown in Figure 7-10. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of RESET TDRT msec after MCLR goes high.

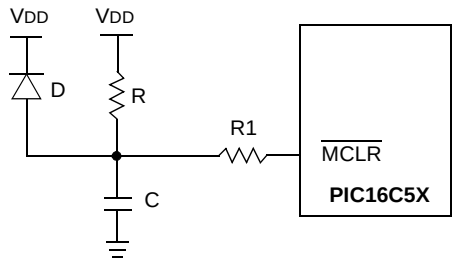
In Figure 7-11, the on-chip Power-on Reset feature is being used (MCLR and VDD are tied together). The VDD is stable before the start-up timer times out and there is no problem in getting a proper RESET. However, Figure 7-12 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses a high on the MCLR/VPP pin, and when the MCLR/VPP pin (and VDD) actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip is, therefore, not guaranteed to function correctly. For such situations, we recommend that external (RESET) BOR circuits or external RC circuits be used to achieve longer POR delay times (Figure 7-9).

Note:	When the device starts normal operation (exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For more information on PIC16C5X POR, see *Power-Up Considerations* - AN522 in the Embedded Control Handbook.

The POR circuit does not produce an internal RESET when VDD declines.

FIGURE 7-9: EXAMPLE OF EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- External Power-on Reset circuit is required only if VDD power-up is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- R < 40 kΩ is recommended to make sure that voltage drop across R does not violate the device electrical specification.
- R1 = 100Ω to 1 kΩ will limit any current flowing into MCLR from external capacitor C in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

FIGURE 7-10: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ NOT TIED TO V_{DD})

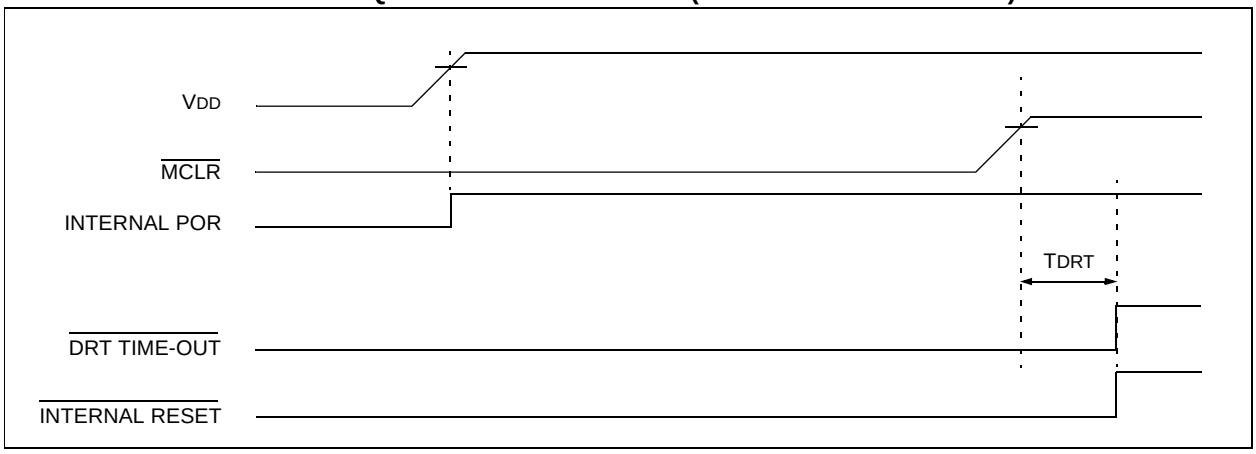


FIGURE 7-11: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): FAST V_{DD} RISE TIME

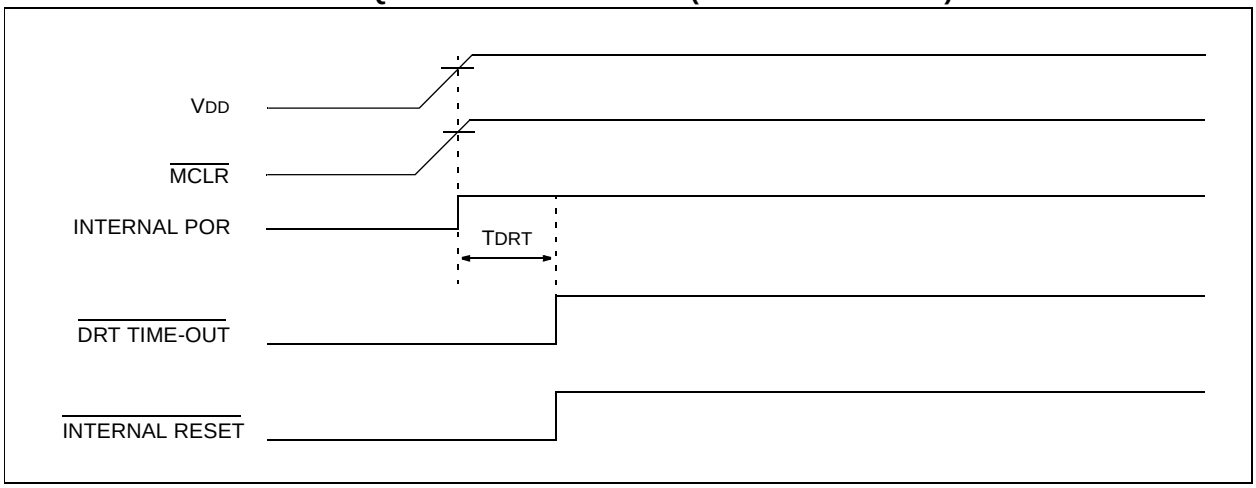
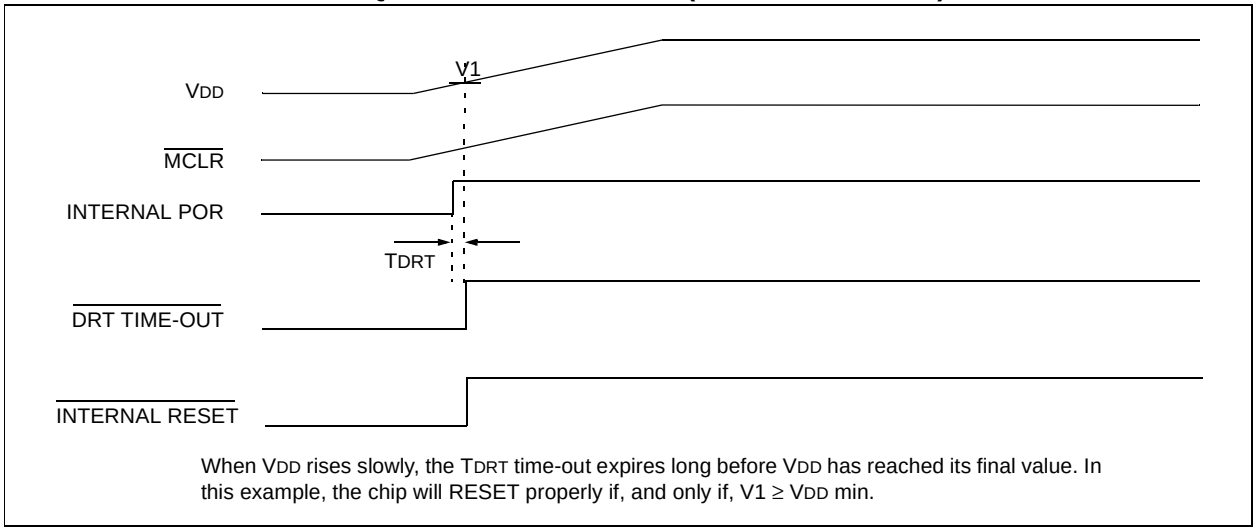


FIGURE 7-12: TIME-OUT SEQUENCE ON POWER-UP ($\overline{MCLR}$ TIED TO V_{DD}): SLOW V_{DD} RISE TIME



When V_{DD} rises slowly, the T_{DRT} time-out expires long before V_{DD} has reached its final value. In this example, the chip will RESET properly if, and only if, V1 ≥ V_{DD} min.

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7.5 Device Reset Timer (DRT)

The Device Reset Timer (DRT) provides a fixed 18 ms nominal time-out on RESET. The DRT operates on an internal RC oscillator. The processor is kept in RESET as long as the DRT is active. The DRT delay allows V_{DD} to rise above V_{DD} min., and for the oscillator to stabilize.

Oscillator circuits based on crystals or ceramic resonators require a certain time after power-up to establish a stable oscillation. The on-chip DRT keeps the device in a RESET condition for approximately 18 ms after the voltage on the $\overline{MCLR}/V_{PP}$ pin has reached a logic high (V_{IH}) level. Thus, external RC networks connected to the $\overline{MCLR}$ input are not required in most cases, allowing for savings in cost-sensitive and/or space restricted applications.

The Device Reset time delay will vary from device to device due to V_{DD}, temperature, and process variation. See AC parameters for details.

The DRT will also be triggered upon a Watchdog Timer time-out. This is particularly important for applications using the WDT to wake the PIC16C5X from SLEEP mode automatically.

7.6 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKIN pin. That means that the WDT will run even if the clock on the OSC1/CLKIN and OSC2/CLKOUT pins have been stopped, for example, by execution of a SLEEP instruction. During normal operation or SLEEP, a WDT Reset or Wake-up Reset generates a device RESET.

The $\overline{TO}$ bit (STATUS<4>) will be cleared upon a Watchdog Timer Reset.

The WDT can be permanently disabled by programming the configuration bit WDTE as a '0' (Section 7.1). Refer to the PIC16C5X Programming Specifications (Literature Number DS30190) to determine how to access the configuration word.

7.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms (with no prescaler). If a longer time-out period is desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT (under software control) by writing to the OPTION register. Thus, a time-out period of a nominal 2.3 seconds can be realized. These periods vary with temperature, V_{DD} and part-to-part process variations (see DC specs).

Under worst case conditions (V_{DD} = Min., Temperature = Max., max. WDT prescaler), it may take several seconds before a WDT time-out occurs.

7.6.2 WDT PROGRAMMING CONSIDERATIONS

The `CLRWDT` instruction clears the WDT and the postscaler, if assigned to the WDT, and prevents it from timing out and generating a device RESET.

The `SLEEP` instruction resets the WDT and the postscaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

FIGURE 7-13: WATCHDOG TIMER BLOCK DIAGRAM

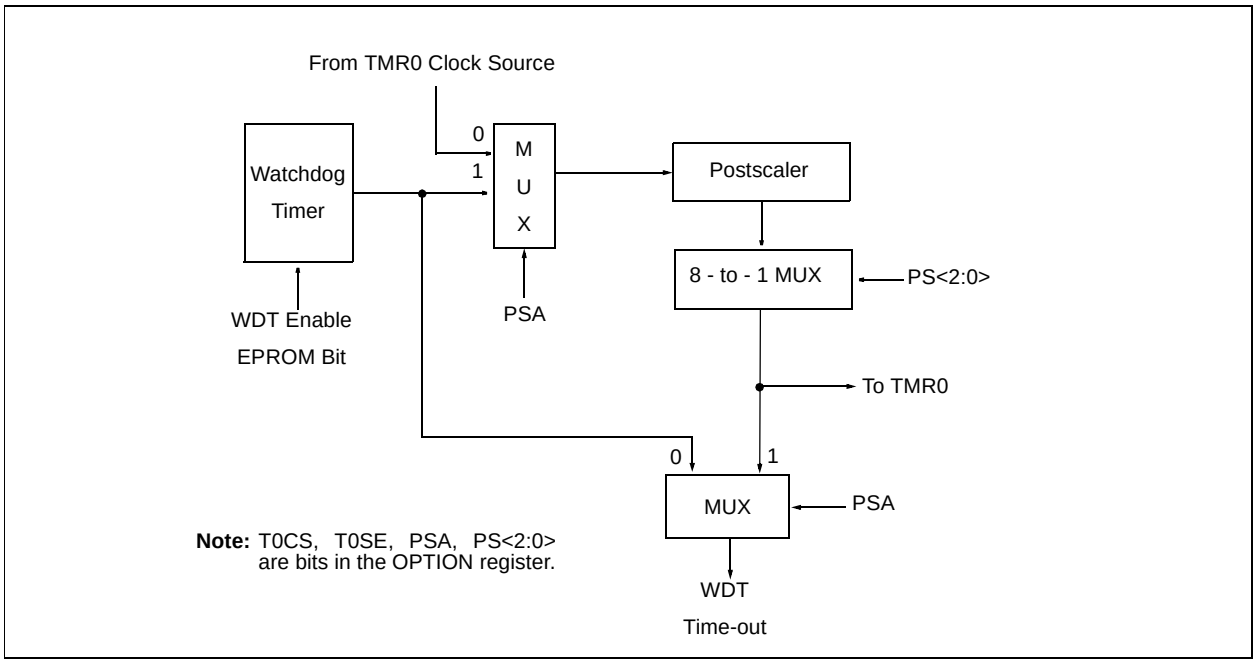

TABLE 7-5: SUMMARY OF REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-on Reset	Value on MCLR and WDT Reset
N/A	OPTION	—	—	T0CS	T0SE	PSA	PS2	PS1	PS0	--11 1111	--11 1111

Legend: Shaded boxes = Not used by Watchdog Timer, - = unimplemented, read as '0', u = unchanged

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7.7 Time-Out Sequence and Power-down Status Bits (TO/PD)

The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be tested to determine if a RESET condition has been caused by a power-up condition, a $\overline{MCLR}$ or Watchdog Timer (WDT) Reset, or a $\overline{MCLR}$ or WDT Wake-up Reset.

TABLE 7-6: $\overline{TO}$/$\overline{PD}$ STATUS AFTER RESET

$\overline{TO}$	$\overline{PD}$	RESET was caused by
1	1	Power-up (POR)
u	u	$\overline{MCLR}$ Reset (normal operation)(1)
1	0	$\overline{MCLR}$ Wake-up Reset (from SLEEP)
0	1	WDT Reset (normal operation)
0	0	WDT Wake-up Reset (from SLEEP)

Legend: u = unchanged

Note 1: The $\overline{TO}$ and $\overline{PD}$ bits maintain their status (u) until a RESET occurs. A low-pulse on the $\overline{MCLR}$ input does not change the $\overline{TO}$ and $\overline{PD}$ status bits.

These STATUS bits are only affected by events listed in Table 7-7.

TABLE 7-7: EVENTS AFFECTING $\overline{TO}$/$\overline{PD}$ STATUS BITS

Event	$\overline{TO}$	$\overline{PD}$	Remarks
Power-up	1	1	
WDT Time-out	0	u	No effect on $\overline{PD}$
SLEEP instruction	1	0	
CLRWDT instruction	1	1	

Legend: u = unchanged

Note: A WDT time-out will occur regardless of the status of the $\overline{TO}$ bit. A SLEEP instruction will be executed, regardless of the status of the $\overline{PD}$ bit.

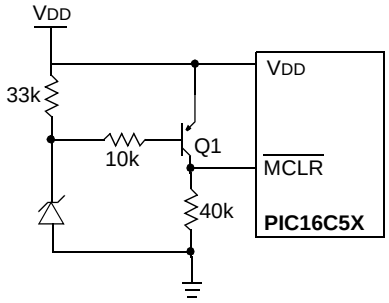
Table 7-3 lists the RESET conditions for the Special Function Registers, while Table 7-4 lists the RESET conditions for all the registers.

7.8 RESET on Brown-Out

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out.

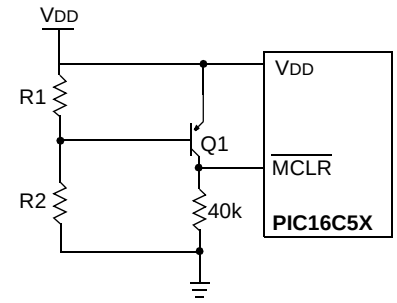
To reset PIC16C5X devices when a brown-out occurs, external brown-out protection circuits may be built, as shown in Figure 7-14 and Figure 7-15.

FIGURE 7-14: BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate RESET when V_{DD} goes below Vz + 0.7V (where Vz = Zener voltage).

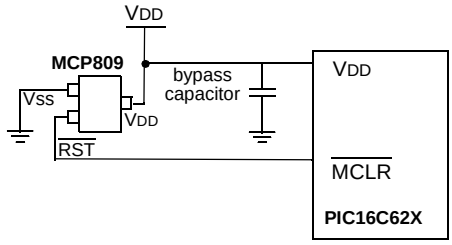
FIGURE 7-15: BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, although less accurate. Transistor Q1 turns off when V_{DD} is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

FIGURE 7-16: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 3



This brown-out protection circuit employs Microchip Technology's MCP809 microcontroller supervisor. The MCP8XX and MCP1XX families of supervisors provide push-pull and open collector outputs with both "active high and active low" RESET pins. There are 7 different trip point selections to accommodate 5V and 3V systems.

7.9 Power-down Mode (SLEEP)

A device may be powered down (SLEEP) and later powered up (wake-up from SLEEP).

7.9.1 SLEEP

The Power-down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit (STATUS<4>) is set, the $\overline{PD}$ bit (STATUS<3>) is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low, or hi-impedance).

It should be noted that a RESET generated by a WDT time-out does not drive the $\overline{MCLR}/V_{PP}$ pin low.

For lowest current consumption while powered down, the T0CKI input should be at V_{DD} or V_{SS} and the $\overline{MCLR}/V_{PP}$ pin must be at a logic high level.

7.9.2 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. An external RESET input on $\overline{MCLR}/V_{PP}$ pin.
2. A Watchdog Timer time-out RESET (if WDT was enabled).

Both of these events cause a device RESET. The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of device RESET. The $\overline{TO}$ bit is cleared if a WDT time-out occurred (and caused wake-up). The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked.

The WDT is cleared when the device wakes from SLEEP, regardless of the wake-up source.

7.10 Program Verification/Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note:	Microchip does not recommend code protecting windowed devices.

7.11 ID Locations

Four memory locations are designated as ID locations, where the user can store checksum or other code-identification numbers. These locations are not accessible during normal execution but are readable and writable during program/verify.

Use only the lower 4 bits of the ID locations and always program the upper 8 bits as '1's.

Note:	Microchip will assign a unique pattern number for QTP and SQTP requests and for ROM devices. This pattern number will be unique and traceable to the submitted code.

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8.0 INSTRUCTION SET SUMMARY

Each PIC16C5X instruction is a 12-bit word divided into an OPCODE, which specifies the instruction type, and one or more operands which further specify the operation of the instruction. The PIC16C5X instruction set summary in Table 8-2 groups the instructions into byte-oriented, bit-oriented, and literal and control operations. Table 8-1 shows the opcode field descriptions.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator is used to specify which one of the 32 file registers in that bank is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 8-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top of Stack
PC	Program Counter
WDT	Watchdog Timer Counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
→	Assigned to
< >	Register bit field
∈	In the set of
italics	User defined term (font is courier)

All instructions are executed within one single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time would be 1 µs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time would be 2 µs.

Figure 8-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 8-1: GENERAL FORMAT FOR INSTRUCTIONS

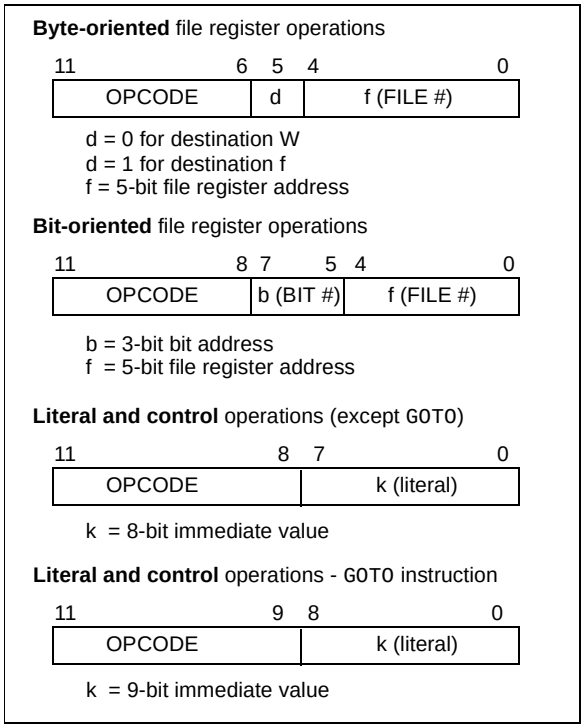

TABLE 8-2: INSTRUCTION SET SUMMARY

Mnemonic, Operands		Description	Cycles	12-Bit Opcode MSb	LSb	Status Affected	Notes
ADDWF	**f,d**	Add W and f	1	0001	11df ffff	C,DC,Z	1,2,4
ANDWF	**f,d**	AND W with f	1	0001	01df ffff	Z	2,4
CLRF	**f**	Clear f	1	0000	011f ffff	Z	4
CLRW	**–**	Clear W	1	0000	0100 0000	Z	
COMF	**f, d**	Complement f	1	0010	01df ffff	Z	
DECF	**f, d**	Decrement f	1	0000	11df ffff	Z	2,4
DECFSZ	**f, d**	Decrement f, Skip if 0	1(2)	0010	11df ffff	None	2,4
INCF	**f, d**	Increment f	1	0010	10df ffff	Z	2,4
INCFSZ	**f, d**	Increment f, Skip if 0	1(2)	0011	11df ffff	None	2,4
IORWF	**f, d**	Inclusive OR W with f	1	0001	00df ffff	Z	2,4
MOVF	**f, d**	Move f	1	0010	00df ffff	Z	2,4
MOVWF	**f**	Move W to f	1	0000	001f ffff	None	1,4
NOP	**–**	No Operation	1	0000	0000 0000	None	
RLF	**f, d**	Rotate left f through Carry	1	0011	01df ffff	C	2,4
RRF	**f, d**	Rotate right f through Carry	1	0011	00df ffff	C	2,4
SUBWF	**f, d**	Subtract W from f	1	0000	10df ffff	C,DC,Z	1,2,4
SWAPF	**f, d**	Swap f	1	0011	10df ffff	None	2,4
XORWF	**f, d**	Exclusive OR W with f	1	0001	10df ffff	Z	2,4
BIT-ORIENTED FILE REGISTER OPERATIONS							
BCF	**f, b**	Bit Clear f	1	0100	bbbf ffff	None	2,4
BSF	**f, b**	Bit Set f	1	0101	bbbf ffff	None	2,4
BTFSC	**f, b**	Bit Test f, Skip if Clear	1 (2)	0110	bbbf ffff	None	
BTFSS	**f, b**	Bit Test f, Skip if Set	1 (2)	0111	bbbf ffff	None	
LITERAL AND CONTROL OPERATIONS							
ANDLW	**k**	AND literal with W	1	1110	kkkk kkkk	Z	
CALL	**k**	Call subroutine	2	1001	kkkk kkkk	None	1
CLRWDT	**k**	Clear Watchdog Timer	1	0000	0000 0100	$\overline{TO}$, $\overline{PD}$	
GOTO	**k**	Unconditional branch	2	101k	kkkk kkkk	None	
IORLW	**k**	Inclusive OR Literal with W	1	1101	kkkk kkkk	Z	
MOVLW	**k**	Move Literal to W	1	1100	kkkk kkkk	None	
OPTION	**k**	Load OPTION register	1	0000	0000 0010	None	
RETLW	**k**	Return, place Literal in W	2	1000	kkkk kkkk	None	
SLEEP	**–**	Go into standby mode	1	0000	0000 0011	$\overline{TO}$, $\overline{PD}$	
TRIS	**f**	Load TRIS register	1	0000	0000 0fff	None	3
XORLW	**k**	Exclusive OR Literal to W	1	1111	kkkk kkkk	Z	

Note 1: The 9th bit of the program counter will be forced to a '0' by any instruction that writes to the PC except for GOTO. (See individual device data sheets, Memory Section/Indirect Data Addressing, INDF and FSR Registers)

2: When an I/O register is modified as a function of itself (e.g. MOVF PORTB, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

3: The instruction TRIS f, where f = 5 or 6 causes the contents of the W register to be written to the tristate latches of PORTA or B respectively. A '1' forces the pin to a hi-impedance state and disables the output buffers.

4: If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared (if assigned to TMR0).

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ADDWF **Add W and f**

Syntax: [*label*] ADDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) + (f) → (dest)

Status Affected: C, DC, Z

Encoding:

0001	11df	ffff

Description: Add the contents of the W register and register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ADDWF   FSR, 0
```
Before Instruction
W = 0x17
FSR = 0xC2

After Instruction
W = 0xD9
FSR = 0xC2

ANDWF **AND W with f**

Syntax: [*label*] ANDWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .AND. (f) → (dest)

Status Affected: Z

Encoding:

0001	01df	ffff

Description: The contents of the W register are AND'ed with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is '1' the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
ANDWF   FSR,    1
```
Before Instruction
W = 0x17
TEMP_REG = 0xC2

After Instruction
W = 0x17
TEMP_REG = 0x2

ANDLW **And literal with W**

Syntax: [*label*] ANDLW k

Operands: $0 \le k \le 255$

Operation: (W).AND. (k) → (W)

Status Affected: Z

Encoding:

1110	kkkk	kkkk

Description: The contents of the W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
ANDLW   0x5F
```
Before Instruction
W = 0xA3

After Instruction
W = 0x03

BCF **Bit Clear f**

Syntax: [*label*] BCF f,b

Operands: $0 \le f \le 31$
$0 \le b \le 7$

Operation: 0 → (f<b>)

Status Affected: None

Encoding:

0100	bbbf	ffff

Description: Bit 'b' in register 'f' is cleared.

Words: 1

Cycles: 1

Example:
```
BCF     FLAG_REG,  7
```
Before Instruction
FLAG_REG = 0xC7

After Instruction
FLAG_REG = 0x47

BSF **Bit Set f**

Syntax: [*label*] BSF f,b

Operands: 0 ≤ f ≤ 31
0 ≤ b ≤ 7

Operation: 1 → (f<b>)

Status Affected: None

Encoding:

0101	bbbf	ffff

Description: Bit 'b' in register 'f' is set.

Words: 1

Cycles: 1

Example:
```
BSF     FLAG_REG,   7
```
Before Instruction
FLAG_REG = 0x0A
After Instruction
FLAG_REG = 0x8A

BTFSC **Bit Test f, Skip if Clear**

Syntax: [*label*] BTFSC f,b

Operands: 0 ≤ f ≤ 31
0 ≤ b ≤ 7

Operation: skip if (f<b>) = 0

Status Affected: None

Encoding:

0110	bbbf	ffff

Description: If bit 'b' in register 'f' is 0 then the next instruction is skipped.
If bit 'b' is 0 then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSC   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address (HERE)
After Instruction
if FLAG<1> = 0,
PC = address (TRUE);
if FLAG<1> = 1,
PC = address(FALSE)

BTFSS **Bit Test f, Skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: 0 ≤ f ≤ 31
0 ≤ b < 7

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

0111	bbbf	ffff

Description: If bit 'b' in register 'f' is '1' then the next instruction is skipped.
If bit 'b' is '1', then the next instruction fetched during the current instruction execution, is discarded and a NOP is executed instead, making this a 2-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    BTFSS   FLAG,1
FALSE   GOTO    PROCESS_CODE
TRUE    •
        •
        •
```
Before Instruction
PC = address (HERE)
After Instruction
If FLAG<1> = 0,
PC = address (FALSE);
if FLAG<1> = 1,
PC = address (TRUE)

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CALL **Subroutine Call**

Syntax: [*label*] CALL k

Operands: 0 ≤ k ≤ 255

Operation: (PC) + 1→ Top of Stack;
k → PC<7:0>;
(STATUS<6:5>) → PC<10:9>;
0 → PC<8>

Status Affected: None

Encoding:

1001	kkkk	kkkk

Description: Subroutine call. First, return address (PC+1) is pushed onto the stack. The eight bit immediate address is loaded into PC bits <7:0>. The upper bits PC<10:9> are loaded from STATUS<6:5>, PC<8> is cleared. CALL is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
HERE    CALL    THERE
```
Before Instruction
PC = address (HERE)
After Instruction
PC = address (THERE)
TOS = address (HERE + 1)

CLRF **Clear f**

Syntax: [*label*] CLRF f

Operands: 0 ≤ f ≤ 31

Operation: 00h → (f);
1 → Z

Status Affected: Z

Encoding:

0000	011f	ffff

Description: The contents of register 'f' are cleared and the Z bit is set.

Words: 1

Cycles: 1

Example:
```
CLRF    FLAG_REG
```
Before Instruction
FLAG_REG = 0x5A
After Instruction
FLAG_REG = 0x00
Z = 1

CLRW **Clear W**

Syntax: [*label*] CLRW

Operands: None

Operation: 00h → (W);
1 → Z

Status Affected: Z

Encoding:

0000	0100	0000

Description: The W register is cleared. Zero bit (Z) is set.

Words: 1

Cycles: 1

Example:
```
CLRW
```
Before Instruction
W = 0x5A
After Instruction
W = 0x00
Z = 1

CLRWDT **Clear Watchdog Timer**

Syntax: [*label*] CLRWDT

Operands: None

Operation: 00h → WDT;
0 → $\overline{\text{WDT}}$ prescaler (if assigned);
1 → $\overline{\text{TO}}$;
1 → $\overline{\text{PD}}$

Status Affected: $\overline{\text{TO}}$, $\overline{\text{PD}}$

Encoding:

0000	0000	0100

Description: The CLRWDT instruction resets the WDT. It also resets the prescaler, if the prescaler is assigned to the WDT and not Timer0. Status bits $\overline{\text{TO}}$ and $\overline{\text{PD}}$ are set.

Words: 1

Cycles: 1

Example:
```
CLRWDT
```
Before Instruction
WDT counter = ?
After Instruction
WDT counter = 0x00
WDT prescale = 0
$\overline{\text{TO}}$ = 1
$\overline{\text{PD}}$ = 1

COMF **Complement f**

Syntax: [*label*] COMF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: $(\bar{f}) \rightarrow (dest)$

Status Affected: Z

Encoding:

0010	01df	ffff

Description: The contents of register 'f' are complemented. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
COMF    REG1,0
```
Before Instruction
REG1 = 0x13
After Instruction
REG1 = 0x13
W = 0xEC

DECF **Decrement f**

Syntax: [*label*] DECF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – 1 → (dest)

Status Affected: Z

Encoding:

0000	11df	ffff

Description: Decrement register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example:
```
DECF    CNT,    1
```
Before Instruction
CNT = 0x01
Z = 0
After Instruction
CNT = 0x00
Z = 1

DECFSZ **Decrement f, Skip if 0**

Syntax: [*label*] DECFSZ f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – 1 → d; skip if result = 0

Status Affected: None

Encoding:

0010	11df	ffff

Description: The contents of register 'f' are decremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.
If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE     DECFSZ   CNT, 1
         GOTO     LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address (HERE)
After Instruction
CNT = CNT - 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE+1)

GOTO **Unconditional Branch**

Syntax: [*label*] GOTO k

Operands: $0 \le k \le 511$

Operation: k → PC<8:0>;
STATUS<6:5> → PC<10:9>

Status Affected: None

Encoding:

101k	kkkk	kkkk

Description: GOTO is an unconditional branch. The 9-bit immediate value is loaded into PC bits <8:0>. The upper bits of PC are loaded from STATUS<6:5>. GOTO is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
GOTO THERE
```
After Instruction
PC = address (THERE)

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INCF **Increment f**

Syntax: [*label*] INCF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) + 1 → (dest)

Status Affected: Z

Encoding:

0010	10df	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example:
```
INCF    CNT,    1
```
Before Instruction
CNT = 0xFF
Z = 0

After Instruction
CNT = 0x00
Z = 1

INCFSZ **Increment f, Skip if 0**

Syntax: [*label*] INCFSZ f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) + 1 → (dest), skip if result = 0

Status Affected: None

Encoding:

0011	11df	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

If the result is 0, then the next instruction, which is already fetched, is discarded and a NOP is executed instead making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Example:
```
HERE    INCFSZ    CNT,  1
        GOTO      LOOP
CONTINUE •
         •
         •
```
Before Instruction
PC = address (HERE)

After Instruction
CNT = CNT + 1;
if CNT = 0,
PC = address (CONTINUE);
if CNT ≠ 0,
PC = address (HERE +1)

IORLW **Inclusive OR literal with W**

Syntax: [*label*] IORLW k

Operands: $0 \le k \le 255$

Operation: (W) .OR. (k) → (W)

Status Affected: Z

Encoding:

1101	kkkk	kkkk

Description: The contents of the W register are OR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example:
```
IORLW   0x35
```
Before Instruction
W = 0x9A

After Instruction
W = 0xBF
Z = 0

IORWF **Inclusive OR W with f**

Syntax: [*label*] IORWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W).OR. (f) → (dest)

Status Affected: Z

Encoding:

0001	00df	ffff

Description: Inclusive OR the W register with register 'f'. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.

Words: 1

Cycles: 1

Example:
```
IORWF           RESULT, 0
```
Before Instruction
RESULT = 0x13
W = 0x91

After Instruction
RESULT = 0x13
W = 0x93
Z = 0

MOVF **Move f**

Syntax: [*label*] MOVF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) → (dest)

Status Affected: Z

Encoding:

0010	00df	ffff

Description: The contents of register 'f' is moved to destination 'd'. If 'd' is 0, destination is the W register. If 'd' is 1, the destination is file register 'f'. 'd' is 1 is useful to test a file register since status flag Z is affected.

Words: 1

Cycles: 1

Example:
```
MOVF    FSR,    0
```
After Instruction
W = value in FSR register

MOVLW **Move Literal to W**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: k → (W)

Status Affected: None

Encoding:

1100	kkkk	kkkk

Description: The eight bit literal 'k' is loaded into the W register. The don't cares will assemble as 0s.

Words: 1

Cycles: 1

Example:
```
MOVLW   0x5A
```
After Instruction
W = 0x5A

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \le f \le 31$

Operation: (W) → (f)

Status Affected: None

Encoding:

0000	001f	ffff

Description: Move data from the W register to register 'f'.

Words: 1

Cycles: 1

Example:
```
MOVWF   TEMP_REG
```
Before Instruction
TEMP_REG = 0xFF
W = 0x4F

After Instruction
TEMP_REG = 0x4F
W = 0x4F

NOP **No Operation**

Syntax: [*label*] NOP

Operands: None

Operation: No operation

Status Affected: None

Encoding:

0000	0000	0000

Description: No operation.

Words: 1

Cycles: 1

Example:
```
NOP
```

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OPTION **Load OPTION Register**

Syntax: [*label*] OPTION

Operands: None

Operation: (W) → OPTION

Status Affected: None

Encoding:

0000	0000	0010

Description: The content of the W register is loaded into the OPTION register.

Words: 1

Cycles: 1

Example
```
OPTION
```
Before Instruction
W = 0x07

After Instruction
OPTION = 0x07

RETLW **Return with Literal in W**

Syntax: [*label*] RETLW k

Operands: 0 ≤ k ≤ 255

Operation: k → (W);
TOS → PC

Status Affected: None

Encoding:

1000	kkkk	kkkk

Description: The W register is loaded with the eight bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

Words: 1

Cycles: 2

Example:
```
CALL TABLE ;W contains
           ;table offset
           ;value.
•          ;W now has table
•          ;value.
•
TABLE      ADDWF PC   ;W = offset
           RETLW k1   ;Begin table
           RETLW k2   ;
           •
           •
           •
           RETLW kn   ; End of table
```
Before Instruction
W = 0x07

After Instruction
W = value of k8

RLF **Rotate Left f through Carry**

Syntax: [*label*] RLF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

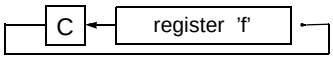
Operation: See description below

Status Affected: C

Encoding:

0011	01df	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example:
```
RLF     REG1,0
```
Before Instruction
```
REG1    =   1110 0110
C       =   0
```
After Instruction
```
REG1    =   1110 0110
W       =   1100 1100
C       =   1
```

RRF **Rotate Right f through Carry**

Syntax: [*label*] RRF f,d

Operands: 0 ≤ f ≤ 31
d ∈ [0,1]

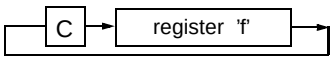
Operation: See description below

Status Affected: C

Encoding:

0011	00df	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0 the result is placed in the W register. If 'd' is 1 the result is placed back in register 'f'.



Words: 1

Cycles: 1

Example:
```
RRF     REG1,0
```
Before Instruction
```
REG1    =   1110 0110
C       =   0
```
After Instruction
```
REG1    =   1110 0110
W       =   0111 0011
C       =   0
```

SLEEP **Enter SLEEP Mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT;
0 → WDT prescaler;
1 → $\overline{TO}$;
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Encoding:

0000	0000	0011

Description: Time-out status bit ($\overline{TO}$) is set. The power-down status bit ($\overline{PD}$) is cleared. The WDT and its prescaler are cleared.

The processor is put into SLEEP mode with the oscillator stopped. See section on SLEEP for more details.

Words: 1

Cycles: 1

Example: SLEEP

SUBWF **Subtract W from f**

Syntax: [*label*] SUBWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f) – (W) → (dest)

Status Affected: C, DC, Z

Encoding:

0000	10df	ffff

Description: Subtract (2's complement method) the W register from register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example 1:

```
SUBWF   REG1, 1
```

Before Instruction
REG1 = 3
W = 2
C = ?

After Instruction
REG1 = 1
W = 2
C = 1 ; result is positive

Example 2:

Before Instruction
REG1 = 2
W = 2
C = ?

After Instruction
REG1 = 0
W = 2
C = 1 ; result is zero

Example 3:

Before Instruction
REG1 = 1
W = 2
C = ?

After Instruction
REG1 = FF
W = 2
C = 0 ; result is negative

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SWAPF **Swap Nibbles in f**

Syntax: [*label*] SWAPF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (f<3:0>) → (dest<7:4>);
(f<7:4>) → (dest<3:0>)

Status Affected: None

Encoding:

0011	10df	ffff

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0 the result is placed in W register. If 'd' is 1 the result is placed in register 'f'.

Words: 1

Cycles: 1

Example
```
SWAPF   REG1,  0
```
Before Instruction
REG1 = 0xA5
After Instruction
REG1 = 0xA5
W = 0X5A

TRIS **Load TRIS Register**

Syntax: [*label*] TRIS f

Operands: f = 5, 6 or 7

Operation: (W) → TRIS register f

Status Affected: None

Encoding:

0000	0000	0fff

Description: TRIS register 'f' (f = 5, 6, or 7) is loaded with the contents of the W register.

Words: 1

Cycles: 1

Example
```
TRIS    PORTA
```
Before Instruction
W = 0XA5
After Instruction
TRISA = 0XA5

XORLW **Exclusive OR literal with W**

Syntax: [*label*] XORLW k

Operands: $0 \le k \le 255$

Operation: (W) .XOR. k → (W)

Status Affected: Z

Encoding:

1111	kkkk	kkkk

Description: The contents of the W register are XOR'ed with the eight bit literal 'k'. The result is placed in the W register.

Words: 1

Cycles: 1

Example
```
XORLW  0xAF
```
Before Instruction
W = 0xB5
After Instruction
W = 0x1A

XORWF **Exclusive OR W with f**

Syntax: [*label*] XORWF f,d

Operands: $0 \le f \le 31$
$d \in [0,1]$

Operation: (W) .XOR. (f) → (dest)

Status Affected: Z

Encoding:

0001	10df	ffff

Description: Exclusive OR the contents of the W register with register 'f'. If 'd' is 0 the result is stored in the W register. If 'd' is 1 the result is stored back in register 'f'.

Words: 1

Cycles: 1

Example
```
XORWF  REG,1
```
Before Instruction
REG = 0xAF
W = 0xB5
After Instruction
REG = 0x1A
W = 0xB5

NOTES:

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9.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM Assembler
  - MPLAB-C17 and MPLAB-C18 C Compilers
  - MPLINK/MPLIB Linker/Librarian
- Simulators
  - MPLAB-SIM Software Simulator
- Emulators
  - MPLAB-ICE Real-Time In-Circuit Emulator
  - ICEPIC™
- In-Circuit Debugger
  - MPLAB-ICD for PIC16F87
- Device Programmers
  - PRO MATE® II Universal Programmer
  - PICSTART® Plus Entry-Level Prototype Programmer
- Low-Cost Demonstration Boards
  - PICDEM-1
  - PICDEM-2
  - PICDEM-3
  - PICDEM-17
  - KEELOQ®

9.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. MPLAB is a Windows®-based application which contains:

- Multiple functionality
  - editor
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
- A full featured editor
- A project manager
- Customizable tool bar and key mapping
- A status bar
- On-line help

MPLAB allows you to:

- Edit your source files (either assembly or ‘C’)
- One touch assemble (or compile) and download to PICmicro tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - object code

The ability to use MPLAB with Microchip’s simulator, MPLAB-SIM, allows a consistent platform and the ability to easily switch from the cost-effective simulator to the full featured emulator with minimal retraining.

9.2 MPASM Assembler

MPASM is a full featured universal macro assembler for all PICmicro MCU’s. It can produce absolute code directly in the form of HEX files for device programmers, or it can generate relocatable objects for MPLINK.

MPASM has a command line interface and a Windows shell and can be used as a standalone application on a Windows 3.x or greater system. MPASM generates relocatable object files, Intel standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file which contains source lines and generated machine code, and a COD file for MPLAB debugging.

MPASM features include:

- MPASM and MPLINK are integrated into MPLAB projects.
- MPASM allows user defined macros to be created for streamlined assembly.
- MPASM allows conditional assembly for multi purpose source files.
- MPASM directives allow complete control over the assembly process.

9.3 MPLAB-C17 and MPLAB-C18 C Compilers

The MPLAB-C17 and MPLAB-C18 Code Development Systems are complete ANSI ‘C’ compilers and integrated development environments for Microchip’s PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

9.4 MPLINK/MPLIB Linker/Librarian

MPLINK is a relocatable linker for MPASM and MPLAB-C17 and MPLAB-C18. It can link relocatable objects from assembly or C source files along with pre-compiled libraries using directives from a linker script.

MPLIB is a librarian for pre-compiled code to be used with MPLINK. When a routine from a library is called from another source file, only the modules that contains that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. MPLIB manages the creation and modification of library files.

MPLINK features include:

- MPLINK works with MPASM and MPLAB-C17 and MPLAB-C18.
- MPLINK allows all memory areas to be defined as sections to provide link-time flexibility.

MPLIB features include:

- MPLIB makes linking easier because single libraries can be included instead of many smaller files.
- MPLIB helps keep code maintainable by grouping related modules together.
- MPLIB commands allow libraries to be created and modules to be added, listed, replaced, deleted, or extracted.

9.5 MPLAB-SIM Software Simulator

The MPLAB-SIM Software Simulator allows code development in a PC host environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file or user-defined key press to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

MPLAB-SIM fully supports symbolic debugging using MPLAB-C17 and MPLAB-C18 and MPASM. The Software Simulator offers the flexibility to develop and debug code outside of the laboratory environment making it an excellent multi-project software development tool.

9.6 MPLAB-ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB-ICE Universal In-Circuit Emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers (MCUs). Software control of MPLAB-ICE is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, “make” and download, and source debugging from a single environment.

Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB-ICE allows expansion to support new PICmicro microcontrollers.

The MPLAB-ICE Emulator System has been designed as a real-time emulation system with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows 3.x/95/98 environment were chosen to best make these features available to you, the end user.

MPLAB-ICE 2000 is a full-featured emulator system with enhanced trace, trigger, and data monitoring features. Both systems use the same processor modules and will operate across the full operating speed range of the PICmicro MCU.

9.7 ICEPIC

ICEPIC is a low-cost in-circuit emulation solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X, and PIC16CXXX families of 8-bit one-time-programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules or daughter boards. The emulator is capable of emulating without target application circuitry being present.

9.8 MPLAB-ICD In-Circuit Debugger

Microchip’s In-Circuit Debugger, MPLAB-ICD, is a powerful, low-cost run-time development tool. This tool is based on the flash PIC16F877 and can be used to develop for this and other PICmicro microcontrollers from the PIC16CXXX family. MPLAB-ICD utilizes the In-Circuit Debugging capability built into the PIC16F87X. This feature, along with Microchip’s In-Circuit Serial Programming protocol, offers cost-effective in-circuit flash programming and debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time. The MPLAB-ICD is also a programmer for the flash PIC16F87X family.

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9.9 PRO MATE II Universal Programmer

The PRO MATE II Universal Programmer is a full-featured programmer capable of operating in stand-alone mode as well as PC-hosted mode. PRO MATE II is CE compliant.

The PRO MATE II has programmable V_{DD} and V_{PP} supplies which allows it to verify programmed memory at V_{DD} min and V_{DD} max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode the PRO MATE II can read, verify or program PICmicro devices. It can also set code-protect bits in this mode.

9.10 PICSTART Plus Entry Level Development System

The PICSTART programmer is an easy-to-use, low-cost prototype programmer. It connects to the PC via one of the COM (RS-232) ports. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

PICSTART Plus supports all PICmicro devices with up to 40 pins. Larger pin count devices such as the PIC16C92X, and PIC17C76X may be supported with an adapter socket. PICSTART Plus is CE compliant.

9.11 PICDEM-1 Low-Cost PICmicro Demonstration Board

The PICDEM-1 is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The users can program the sample microcontrollers provided with the PICDEM-1 board, on a PRO MATE II or PICSTART-Plus programmer, and easily test firmware. The user can also connect the PICDEM-1 board to the MPLAB-ICE emulator and download the firmware to the emulator for testing. Additional prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push-button switches and eight LEDs connected to PORTB.

9.12 PICDEM-2 Low-Cost PIC16CXX Demonstration Board

The PICDEM-2 is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-2 board, on a PRO MATE II programmer or PICSTART-Plus, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-2 board to test firmware. Additional prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push-button switches, a potentiometer for simulated analog input, a Serial EEPROM to demonstrate usage of the I^2C bus and separate headers for connection to an LCD module and a keypad.

9.13 PICDEM-3 Low-Cost PIC16CXXX Demonstration Board

The PICDEM-3 is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with a LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM-3 board, on a PRO MATE II programmer or PICSTART Plus with an adapter socket, and easily test firmware. The MPLAB-ICE emulator may also be used with the PICDEM-3 board to test firmware. Additional prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include an RS-232 interface, push-button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM-3 board is an LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM-3 provides an additional RS-232 interface and Windows 3.1 software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

9.14 PICDEM-17

The PICDEM-17 is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756, PIC17C762, and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included, and the user may erase it and program it with the other sample programs using the PRO MATE II or PICSTART Plus device programmers and easily debug and test the sample code. In addition, PICDEM-17 supports down-loading of programs to and executing out of external FLASH memory on board. The PICDEM-17 is also usable with the MPLAB-ICE or PICMASTER emulator, and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

9.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchips HCS Secure Data Products. The HCS evaluation kit includes an LCD display to show changing codes, a decoder to decode transmissions, and a programming interface to program test transmitters.

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TABLE 9-1: DEVELOPMENT TOOLS FROM MICROCHIP

		PIC12CXXX	PIC14000	PIC16C5X	PIC16C6X	PIC16CXXX	PIC16F62X	PIC16C7X	PIC16C7XX	PIC16C8X	PIC16F8XX	PIC16C9XX	PIC17C4X	PIC17C7XX	PIC18CXX2	24CXX/ 25CXX/ 93CXX	HCSXXX	MCRFXXX	MCP2510
Software Tools	MPLAB® Integrated Development Environment	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓				
	MPLAB® C17 Compiler												✓	✓					
	MPLAB® C18 Compiler														✓				
	MPASM/MPLINK	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Emulators	MPLAB®-ICE	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓				
	ICEPIC™ Low-Cost In-Circuit Emulator	✓		✓	✓	✓		✓	✓	✓		✓							
Debugger	MPLAB®-ICD In-Circuit Debugger				✓*			✓*			✓								
Programmers	PICSTART®Plus Low-Cost Universal Dev. Kit	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓				
	PRO MATE® II Universal Programmer	✓	✓	✓	✓	✓	✓**	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		
Demo Boards and Eval Kits	PICDEM-1			✓		✓		✓†		✓			✓						
	PICDEM-2				✓†			✓†							✓				
	PICDEM-3											✓							
	PICDEM-14A		✓																
	PICDEM-17													✓					
	KEELOQ® Evaluation Kit																✓		
	KEELOQ Transponder Kit																✓		
	microID™ Programmer's Kit																	✓	
	125 kHz microID Developer's Kit																	✓	
	125 kHz Anticollision microID Developer's Kit																	✓	
	13.56 MHz Anticollision microID Developer's Kit																	✓	
	MCP2510 CAN Developer's Kit																		✓

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB®-ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77

** Contact Microchip Technology Inc. for availability date.

† Development tool is available on select devices.

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NOTES:

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10.0 ELECTRICAL CHARACTERISTICS - PIC16C54/55/56/57

Absolute Maximum Ratings†

Ambient Temperature under bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... 0V to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} **(2)** ..... 0V to +14V

Voltage on all other pins with respect to V_{SS} ..... –0.6V to (V_{DD} + 0.6V)

Total Power Dissipation **(1)** ..... 800 mW

Max. Current out of V_{SS} pin ..... 150 mA

Max. Current into V_{DD} pin ..... 100 mA

Max. Current into an input pin (T0CKI only) ..... ±500 μA

Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output Clamp Current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA

Max. Output Current sunk by any I/O pin ..... 25 mA

Max. Output Current sourced by any I/O pin ..... 20 mA

Max. Output Current sourced by a single I/O port (PORTA, B or C) ..... 40 mA

Max. Output Current sunk by a single I/O port (PORTA, B or C) ..... 50 mA

Note 1: Power Dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

2: Voltage spikes below V_{SS} at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA, may cause latch-up. Thus, a series resistor of 50 to 100 Ω should be used when applying a "low" level to the $\overline{MCLR}$ pin rather than pulling this pin directly to V_{SS}.

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

10.1 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD		—			
PIC16C5X-RC		3.0	—	6.25	V	FOSC = DC to 4 MHz
PIC16C5X-XT		3.0	—	6.25	V	FOSC = DC to 4 MHz
PIC16C5X-10		4.5	—	5.5	V	FOSC = DC to 10 MHz
PIC16C5X-HS		4.5	—	5.5	V	FOSC = DC to 20 MHz
PIC16C5X-LP		2.5	—	6.25	V	FOSC = DC to 40 kHz
RAM Data Retention Voltage(2)	VDR		1.5*	—	V	Device in SLEEP Mode
VDD Start Voltage to ensure Power-on Reset	VPOR		VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD	—				
PIC16C5X-RC(4)		—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-XT		—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-10		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
PIC16C5X-HS		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
PIC16C5X-LP		—	15	32	µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power-down Current(5)	IPD					
		—	4.0	12	µA	VDD = 3.0V, WDT enabled
		—	0.6	9	µA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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10.2 DC Characteristics: PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +85°C				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
PIC16C5X-RCI		3.0	—	6.25	V	FOSC = DC to 4 MHz
PIC16C5X-XTI		3.0	—	6.25	V	FOSC = DC to 4 MHz
PIC16C5X-10I		4.5	—	5.5	V	FOSC = DC to 10 MHz
PIC16C5X-HSI		4.5	—	5.5	V	FOSC = DC to 20 MHz
PIC16C5X-LPI		2.5	—	6.25	V	FOSC = DC to 40 kHz
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
PIC16C5X-RCI(4)		—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-XTI		—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-10I		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
PIC16C5X-HSI		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
PIC16C5X-LPI		—	15	40	µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power-down Current(5)	IPD					
		—	4.0	14	µA	VDD = 3.0V, WDT enabled
		—	0.6	12	µA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

10.3 DC Characteristics: PIC16C54/55/56/57-RCE, XTE, 10E, HSE, LPE (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C				
Characteristic	**Sym**	**Min**	**Typ (1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
PIC16C5X-RCE		3.25	—	6.0	V	FOSC = DC to 4 MHz
PIC16C5X-XTE		3.25	—	6.0	V	FOSC = DC to 4 MHz
PIC16C5X-10E		4.5	—	5.5	V	FOSC = DC to 10 MHz
PIC16C5X-HSE		4.5	—	5.5	V	FOSC = DC to 16 MHz
PIC16C5X-LPE		2.5	—	6.0	V	FOSC = DC to 40 kHz
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
PIC16C5X-RCE(4)		—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-XTE		—	1.8	3.3	mA	FOSC = 4 MHz, VDD = 5.5V
PIC16C5X-10E		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
PIC16C5X-HSE		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		—	9.0	20	mA	FOSC = 16 MHz, VDD = 5.5V
PIC16C5X-LPE		—	19	55	µA	FOSC = 32 kHz, VDD = 3.25V, WDT disabled
Power-down Current(5)	IPD					
		—	5.0	22	µA	VDD = 3.25V, WDT enabled
		—	0.8	18	µA	VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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10.4 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Commercial) PIC16C54/55/56/57-RCI, XTI, 10I, HSI, LPI (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS	—	0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS	—	0.15 VDD	V	PIC16C5X-RC only(4)
		VSS	—	0.3 VDD	V	PIC16C5X-XT, 10, HS, LP
Input High Voltage	VIH					
I/O ports		0.45 VDD	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD	—	VDD	V	VDD > 5.5V
MCLR (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	PIC16C5X-RC only(4)
		0.7 VDD	—	VDD	V	PIC16C5X-XT, 10, HS, LP
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(2,3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5			µA	VPIN = VSS + 0.25V
			0.5	+5	µA	VPIN = VDD
T0CKI		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
Output High Voltage	VOH					
I/O ports(3)		VDD – 0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD – 0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

10.5 DC Characteristics: PIC16C54/55/56/57-RC, XT, 10, HS, LP (Extended)

DC Characteristics All Pins Except Power Supply Pins		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature –40°C ≤ TA ≤ +125°C Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		Vss	—	0.15 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		Vss	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		Vss	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		Vss	—	0.15 VDD	V	PIC16C5X-RC only(4)
		Vss	—	0.3 VDD	V	PIC16C5X-XT, 10, HS, LP
Input High Voltage	VIH					
I/O ports		0.45 VDD	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD	—	VDD	V	VDD > 5.5 V
MCLR (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	PIC16C5X-RC only(4)
		0.7 VDD	—	VDD	V	PIC16C5X-XT, 10, HS, LP
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current (2,3)	IIL					**For VDD ≤ 5.5 V**
I/O ports		–1	0.5	+1	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5			µA	VPIN = VSS + 0.25V
			0.5	+5	µA	VPIN = VDD
T0CKI		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3	0.5	+3	µA	VSS ≤ VPIN ≤ VDD, PIC16C5X-XT, 10, HS, LP
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, PIC16C5X-RC
Output High Voltage	VOH					
I/O ports(3)		VDD – 0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD – 0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, PIC16C5X-RC

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For PIC16C5X-RC devices, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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10.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

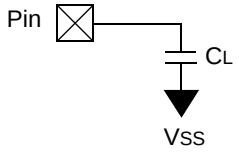
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 10-1: LOAD CONDITIONS - PIC16C54/55/56/57



C_L = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP modes when external clock is used to drive OSC1

10.7 Timing Diagrams and Specifications

FIGURE 10-2: EXTERNAL CLOCK TIMING - PIC16C54/55/56/57

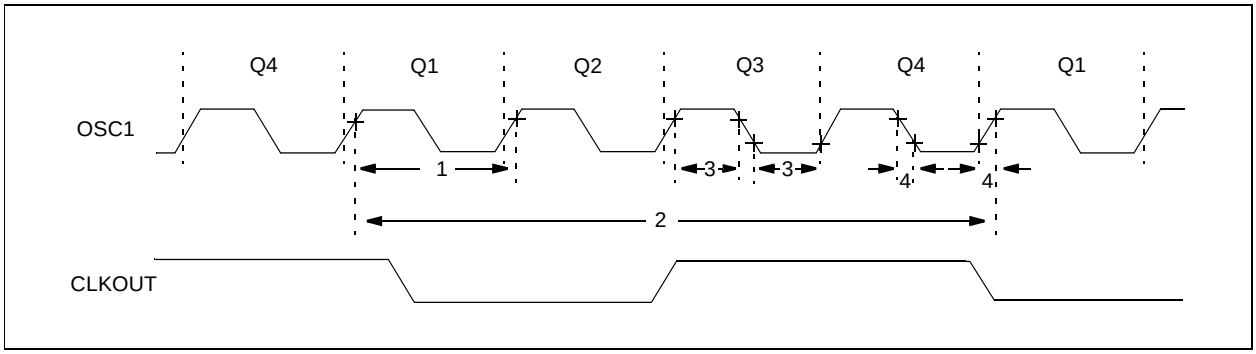


TABLE 10-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	FOSC	External CLKIN Frequency(2)	DC	—	4	MHz	XT osc mode
			DC	—	10	MHz	10 MHz mode
			DC	—	20	MHz	HS osc mode (Com/Indust)
			DC	—	16	MHz	HS osc mode (Extended)
			DC	—	40	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4	MHz	RC osc mode
			0.1	—	4	MHz	XT osc mode
			4	—	10	MHz	10 MHz mode
			4	—	20	MHz	HS osc mode (Com/Indust)
			4	—	16	MHz	HS osc mode (Extended)
			DC	—	40	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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TABLE 10-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54/55/56/57 (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			100	—	—	ns	10 MHz mode
			50	—	—	ns	HS osc mode (Com/Indust)
			62.5	—	—	ns	HS osc mode (Extended)
			25	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			100	—	250	ns	10 MHz mode
			50	—	250	ns	HS osc mode (Com/Indust)
			62.5	—	250	ns	HS osc mode (Extended)
			25	—	—	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

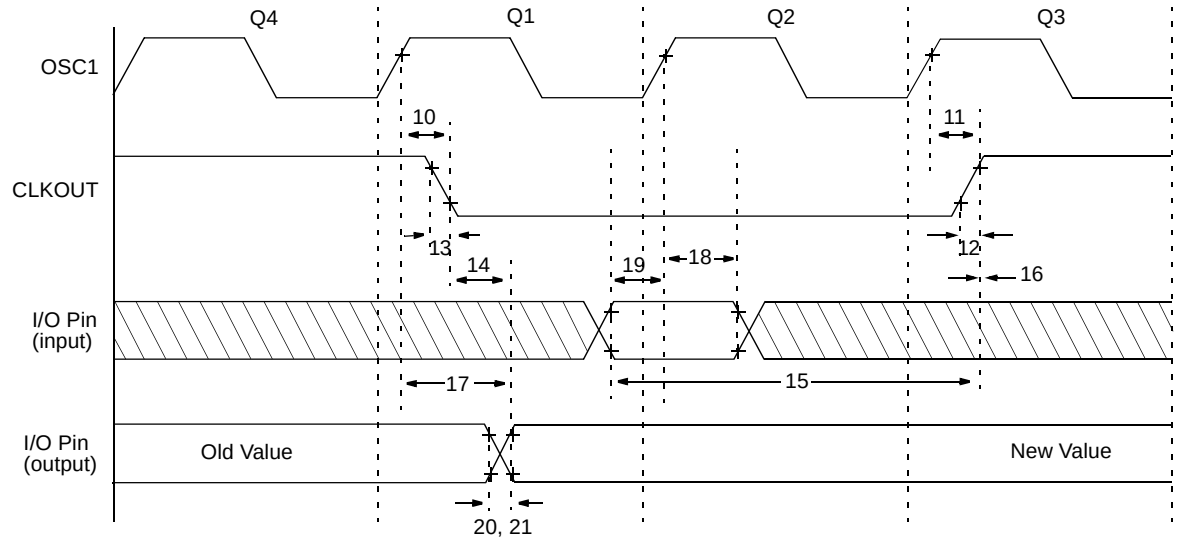
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 10-3: CLKOUT AND I/O TIMING - PIC16C54/55/56/57



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 10-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5	15**	ns
13	TckF	CLKOUT fall time(2)	—	5	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 10-1 for loading conditions.

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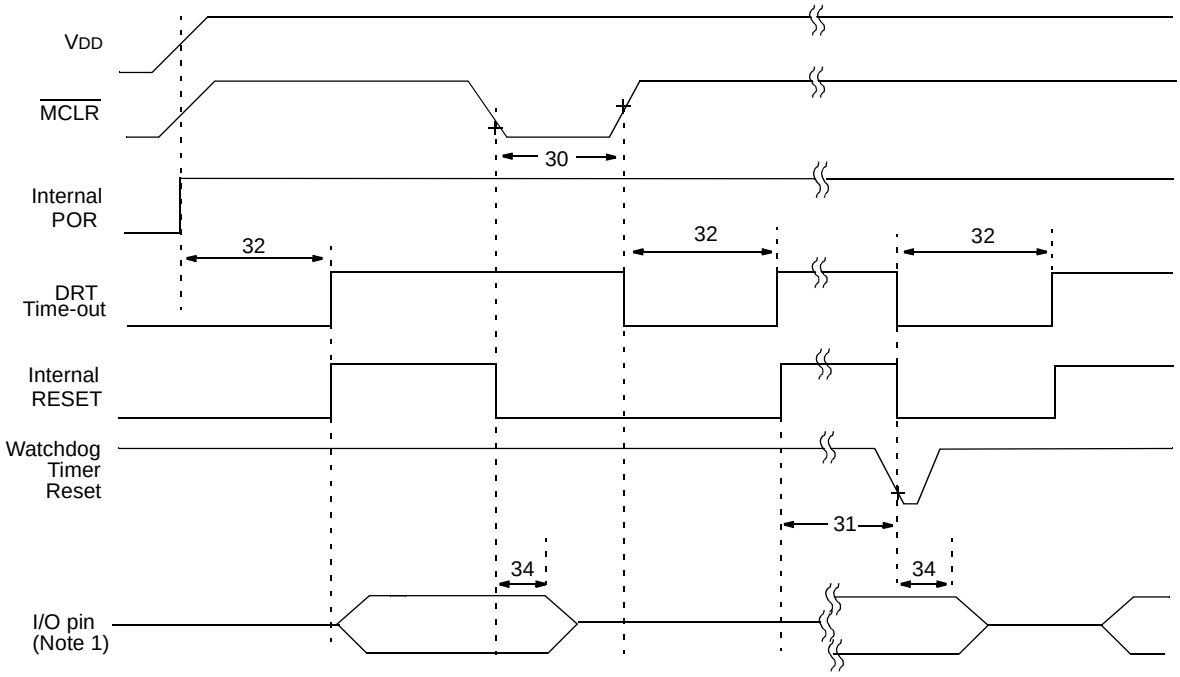
FIGURE 10-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54/55/56/57



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 10-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54/55/56/57

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	100*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9*	18*	30*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 10-5: TIMER0 CLOCK TIMINGS - PIC16C54/55/56/57

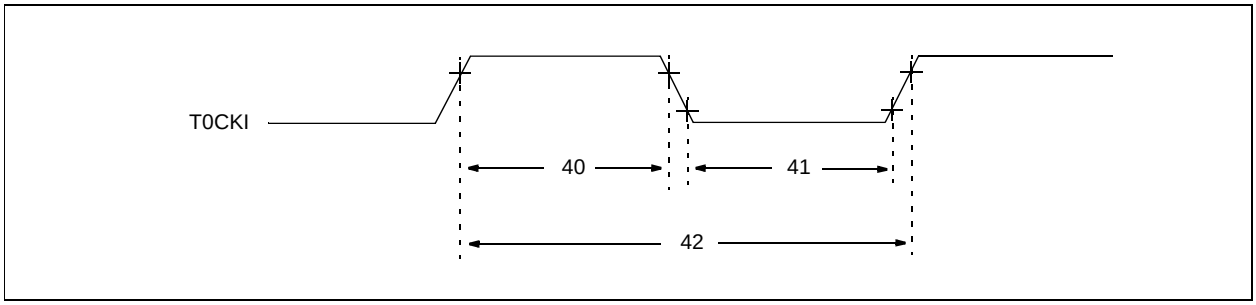


TABLE 10-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54/55/56/57

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width- No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width- No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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11.0 DC AND AC CHARACTERISTICS - PIC16C54/55/56/57

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 11-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

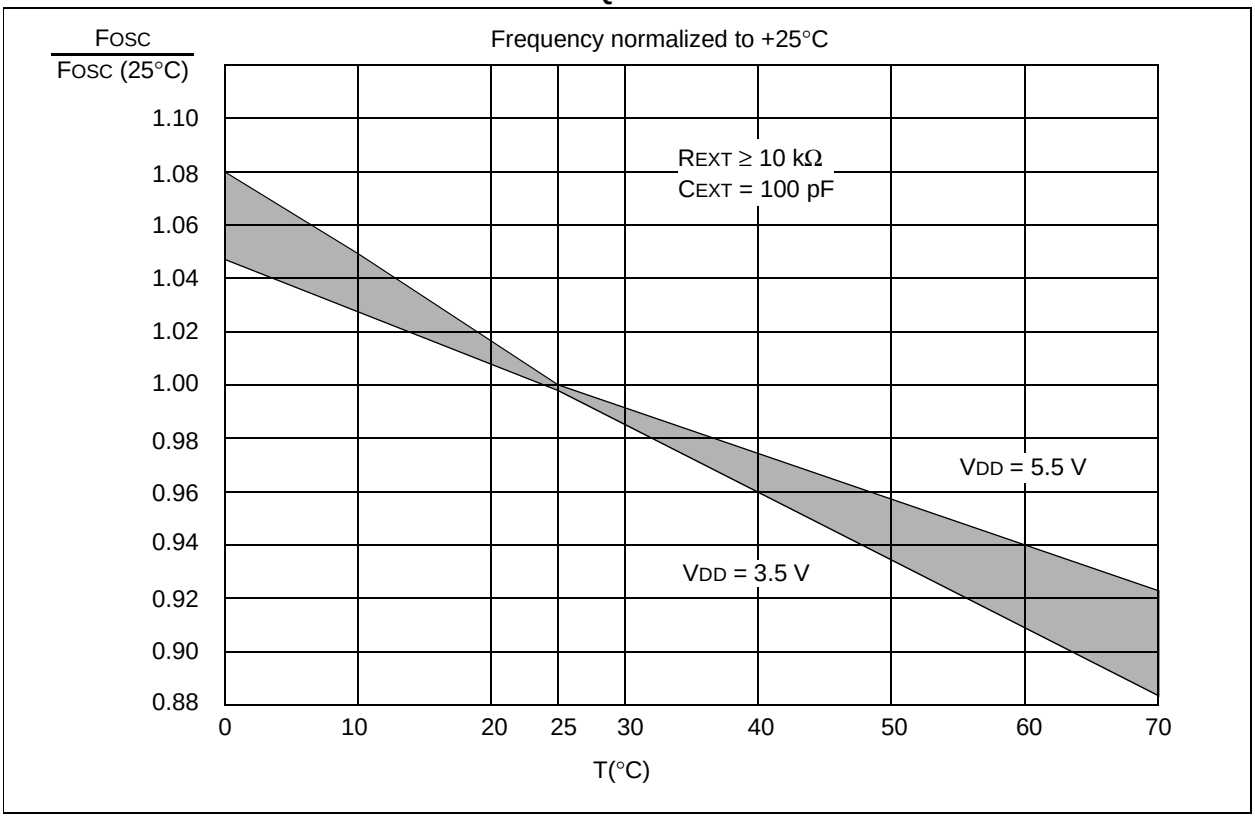

TABLE 11-1: RC OSCILLATOR FREQUENCIES

CEXT	REXT	Average FOSC @ 5 V, 25°C	
20 pF	3.3 k	4.973 MHz	± 27%
	5 k	3.82 MHz	± 21%
	10 k	2.22 MHz	± 21%
	100 k	262.15 kHz	± 31%
100 pF	3.3 k	1.63 MHz	± 13%
	5 k	1.19 MHz	± 13%
	10 k	684.64 kHz	± 18%
	100 k	71.56 kHz	± 25%
300 pF	3.3 k	660 kHz	± 10%
	5.0 k	484.1 kHz	± 14%
	10 k	267.63 kHz	± 15%
	160 k	29.44 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviations from the average value for VDD = 5 V.

FIGURE 11-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF

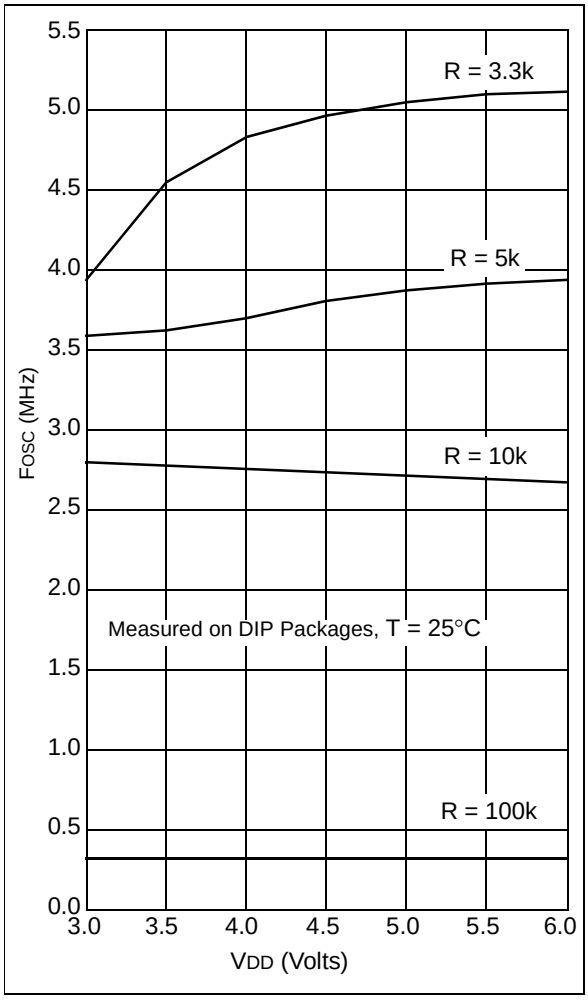

FIGURE 11-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF

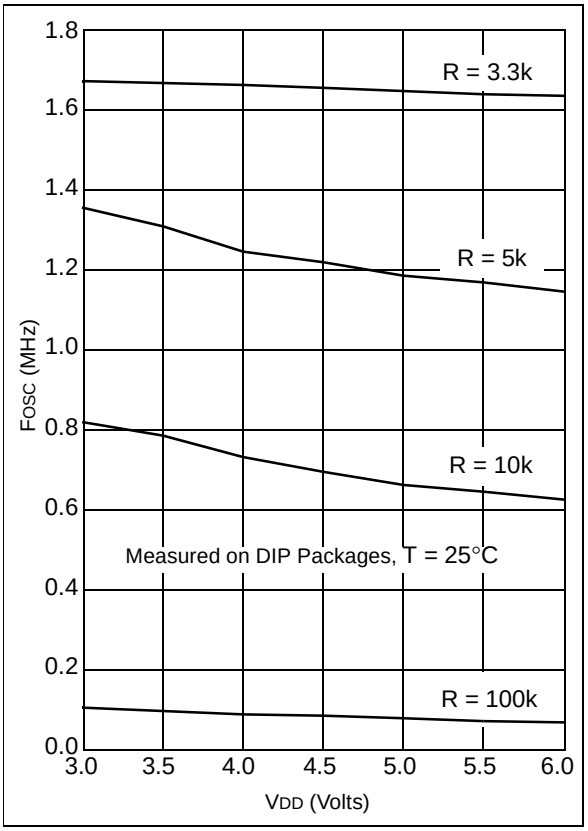

FIGURE 11-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF

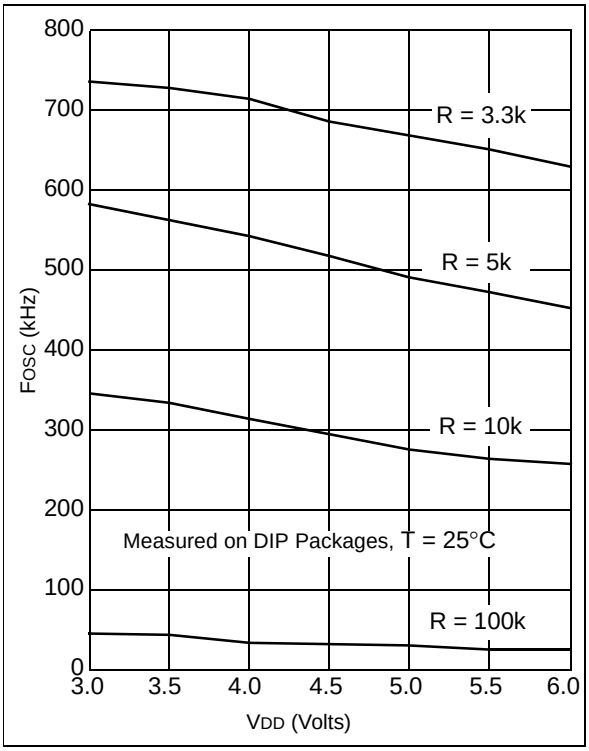

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FIGURE 11-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED

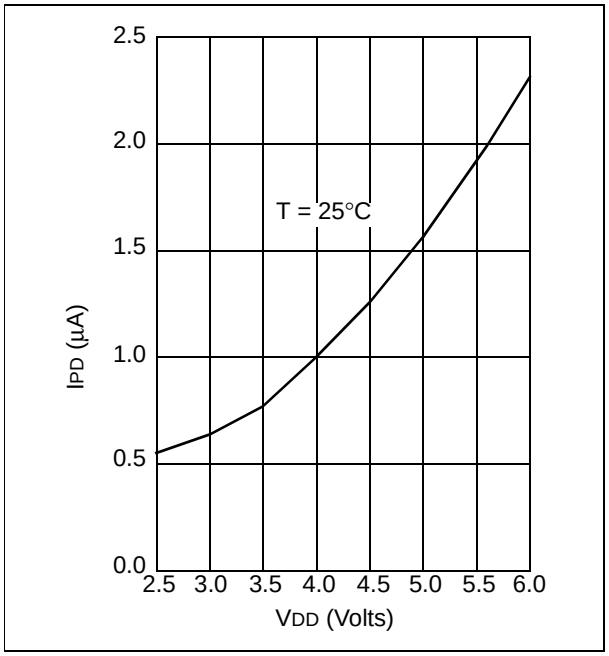


FIGURE 11-6: MAXIMUM IPD vs. VDD, WATCHDOG DISABLED

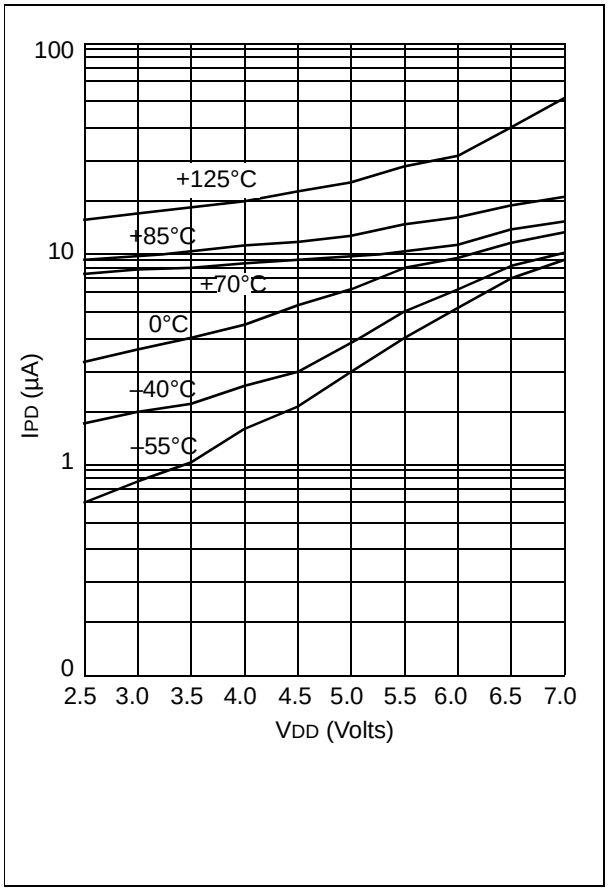


FIGURE 11-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED

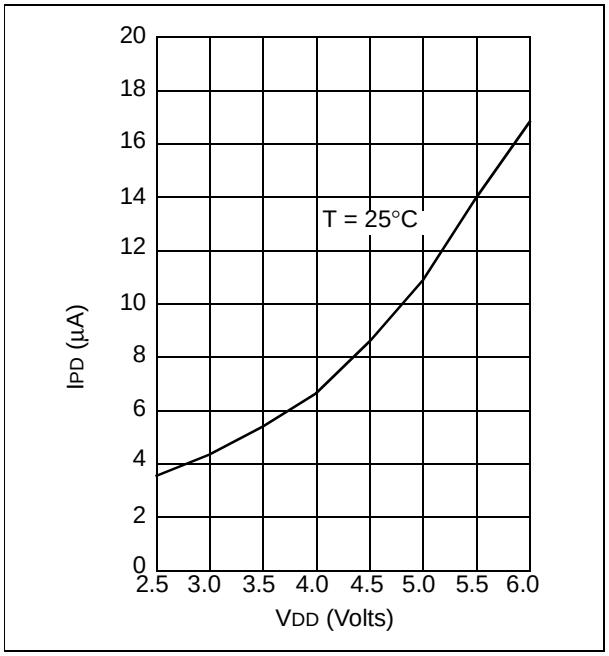
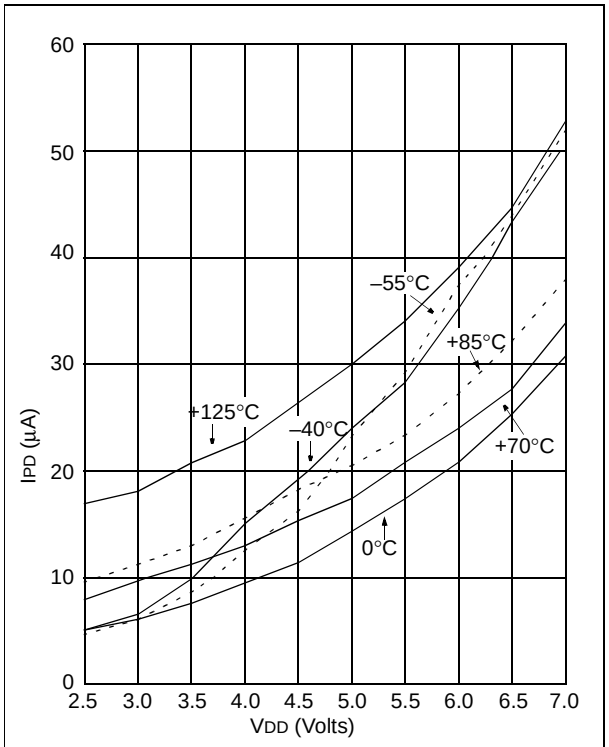


FIGURE 11-8: MAXIMUM IPD vs. VDD, WATCHDOG ENABLED



IPD, with WDT enabled, has two components:
The leakage current, which increases with higher temperature, and the operating current of the WDT logic, which increases with lower temperature. At –40°C, the latter dominates explaining the apparently anomalous behavior.

FIGURE 11-9: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD

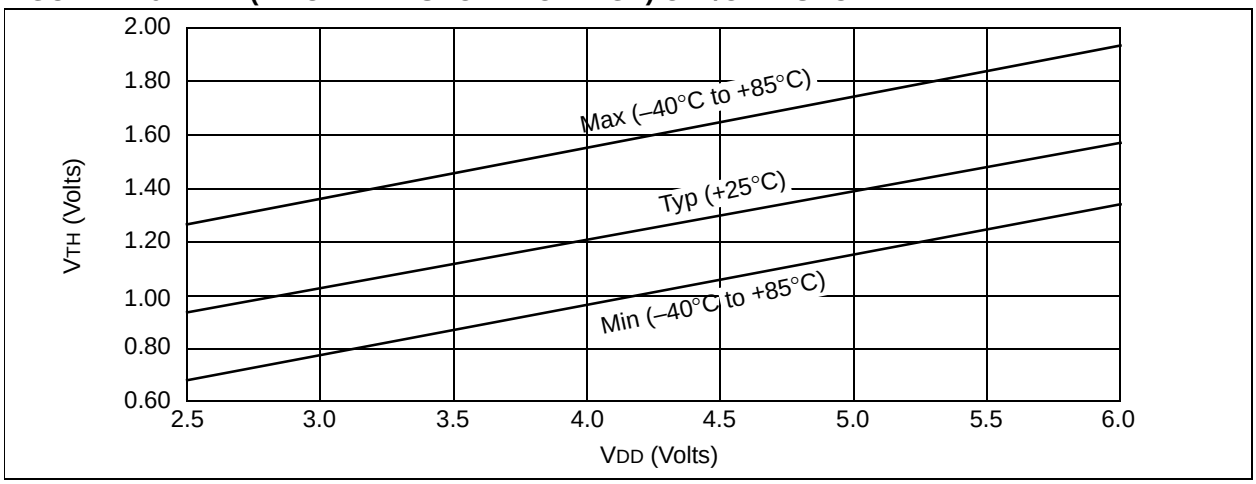
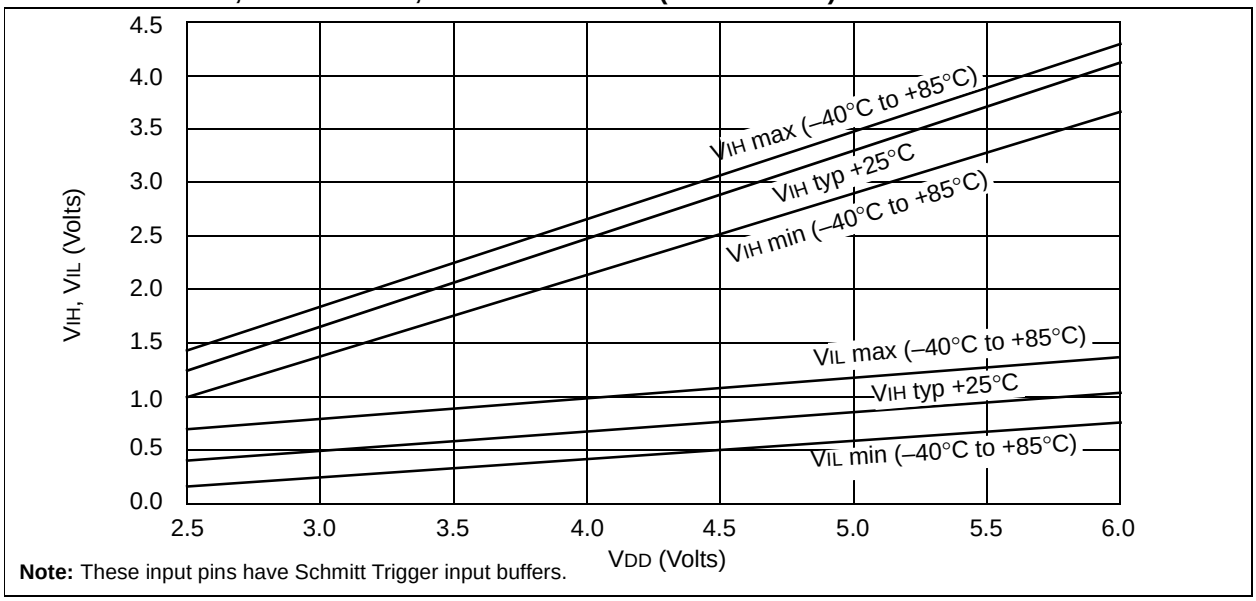


FIGURE 11-10: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (IN RC MODE) vs. VDD



Note: These input pins have Schmitt Trigger input buffers.

FIGURE 11-11: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD

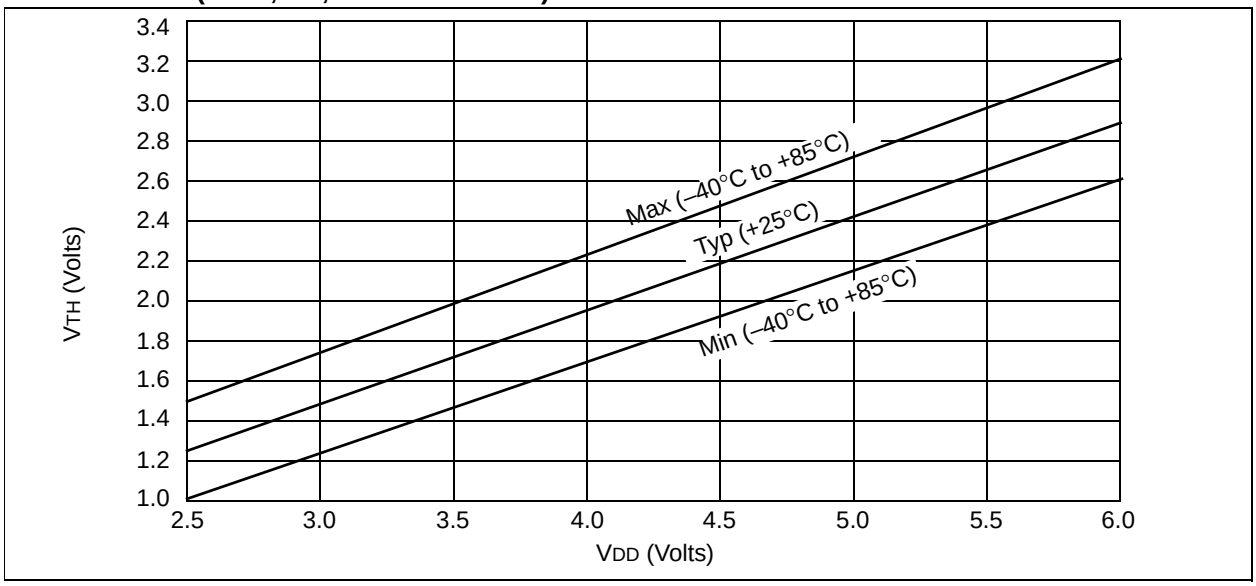


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FIGURE 11-12: TYPICAL IDD vs. FREQUENCY (EXTERNAL CLOCK, 25°C)

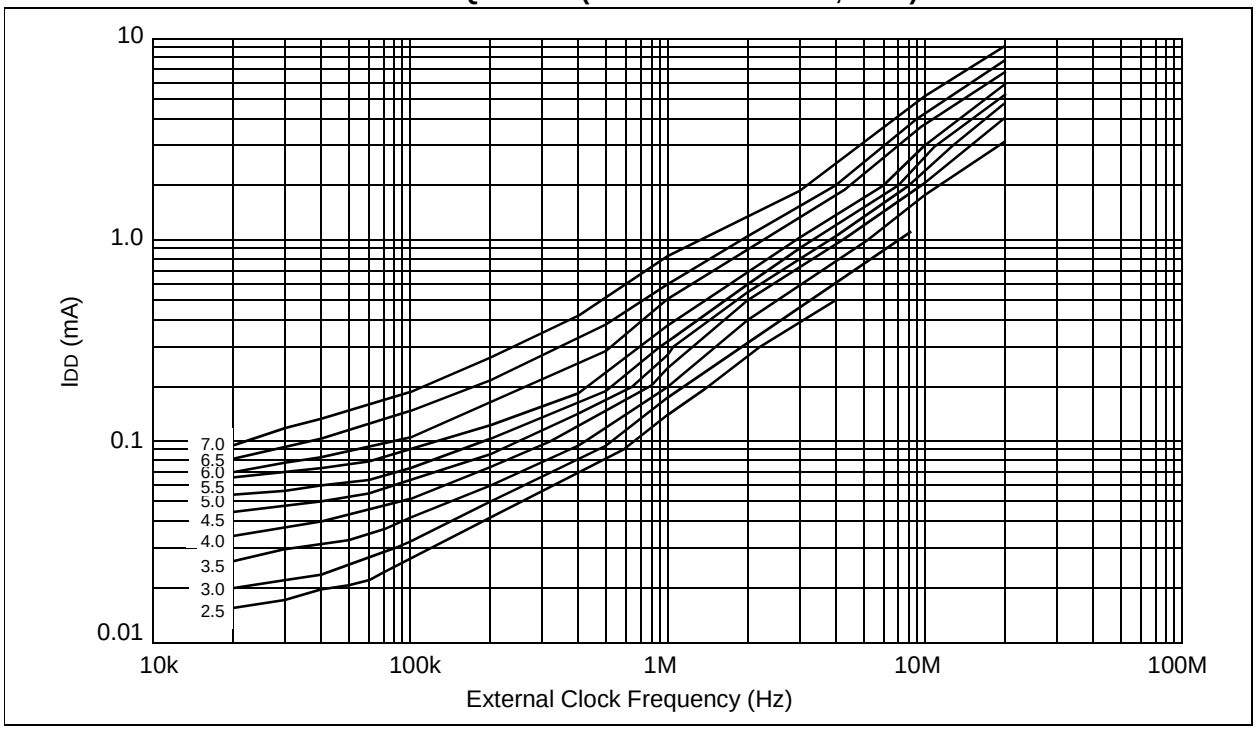

FIGURE 11-13: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK, –40°C TO +85°C)

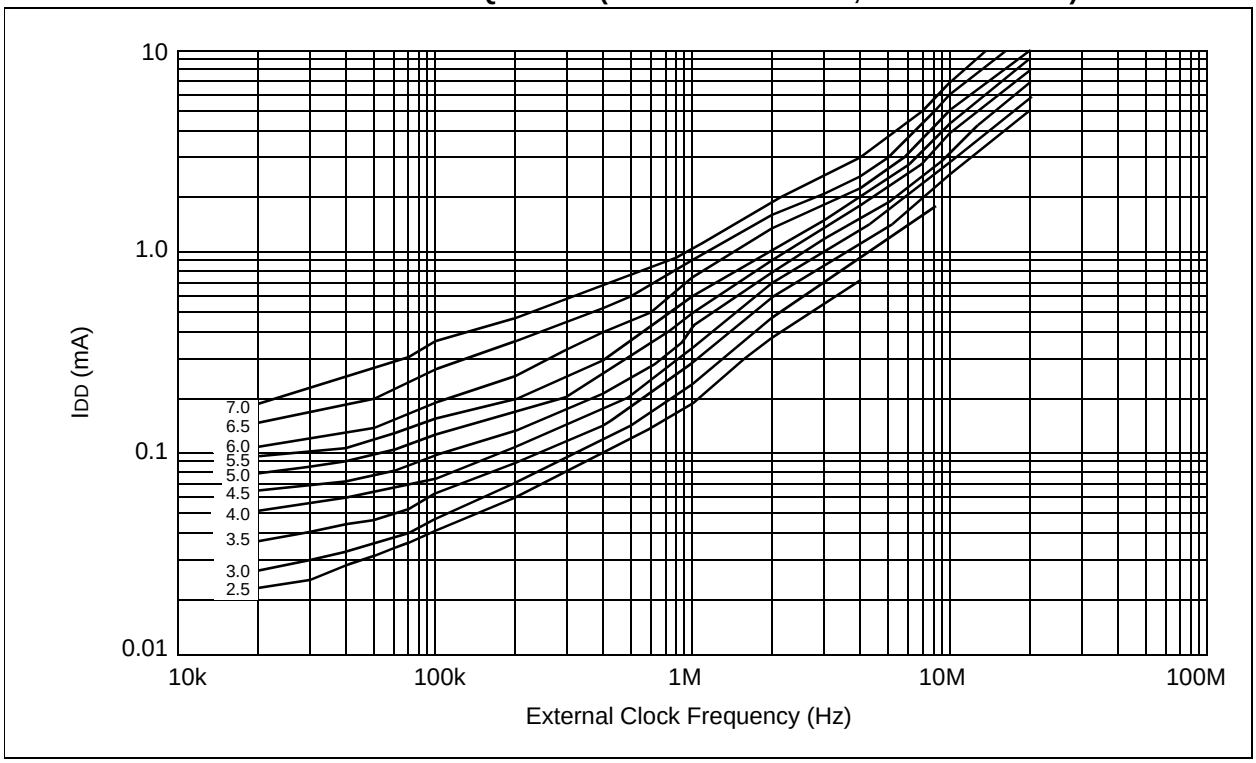

FIGURE 11-14: MAXIMUM IDD vs. FREQUENCY (EXTERNAL CLOCK –55°C TO +125°C)

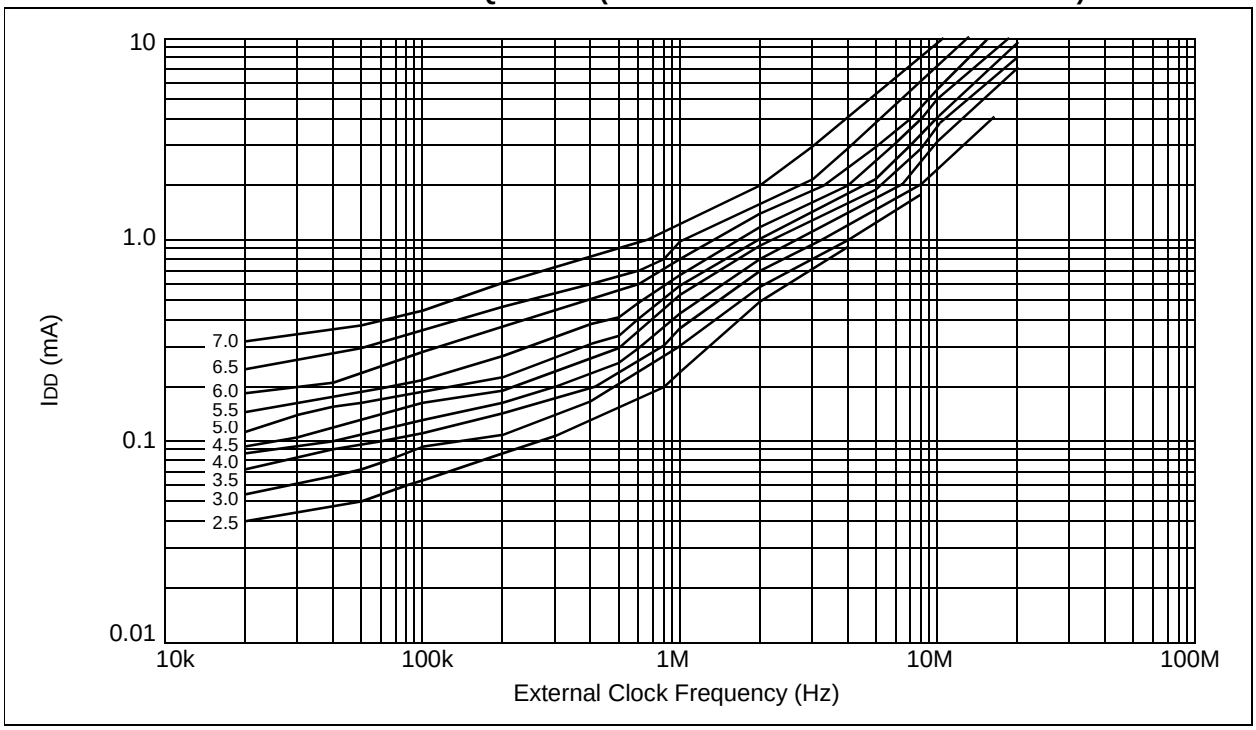

FIGURE 11-15: WDT TIMER TIME-OUT PERIOD vs. VDD

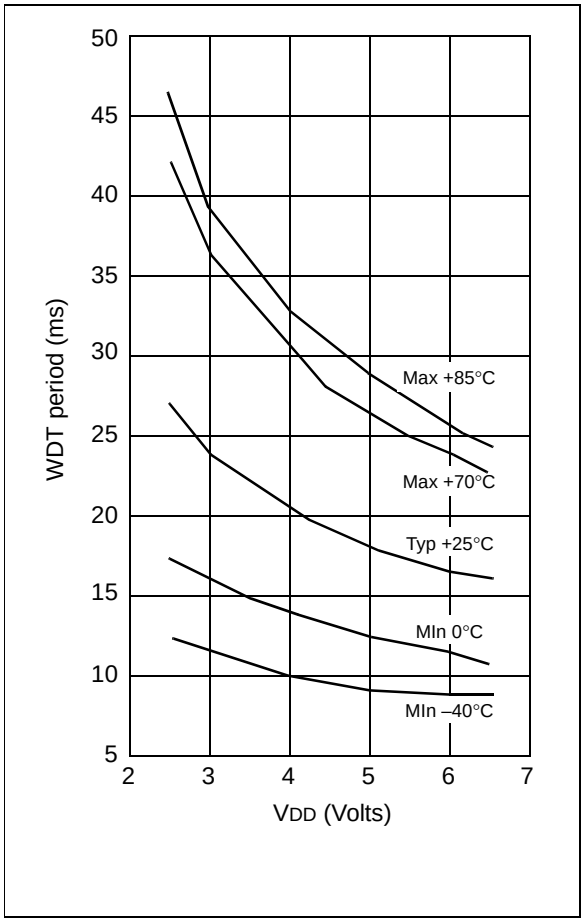

FIGURE 11-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD

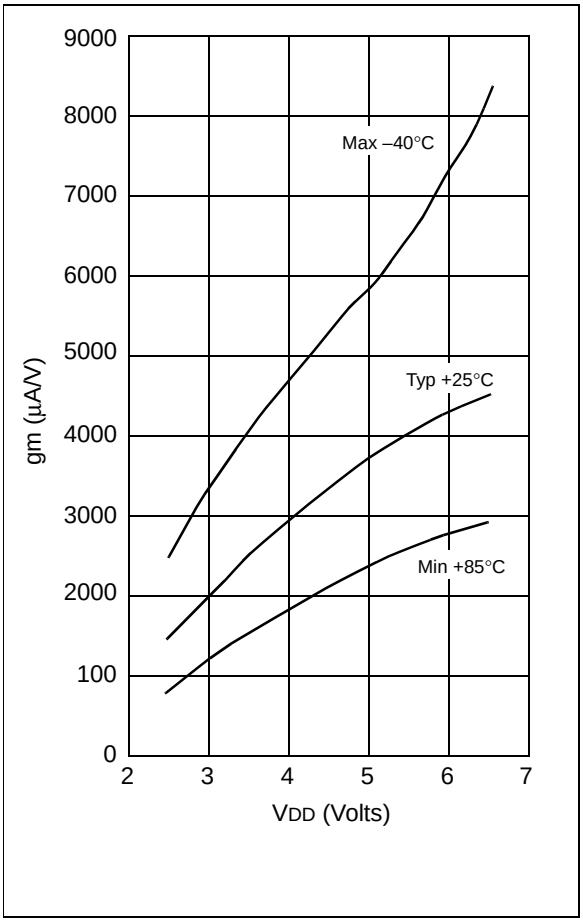

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FIGURE 11-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

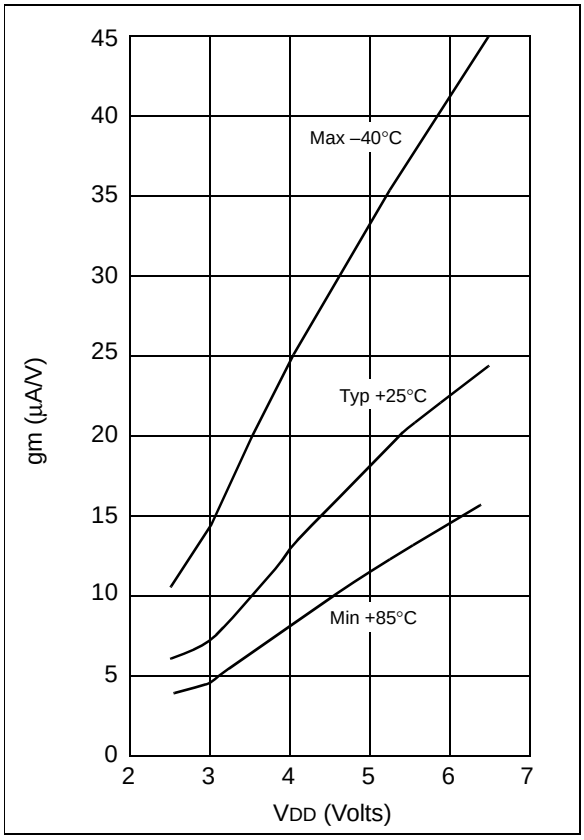

FIGURE 11-18: IOH vs. VOH, VDD = 3 V

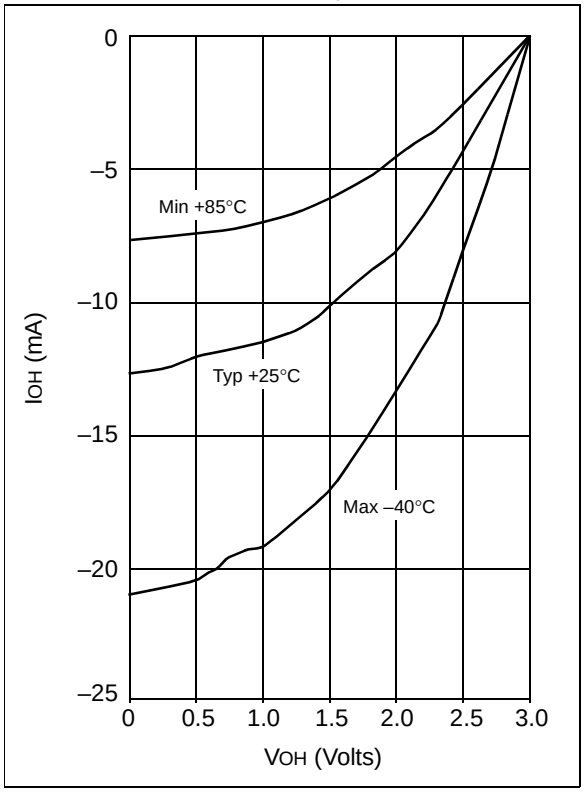

FIGURE 11-19: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

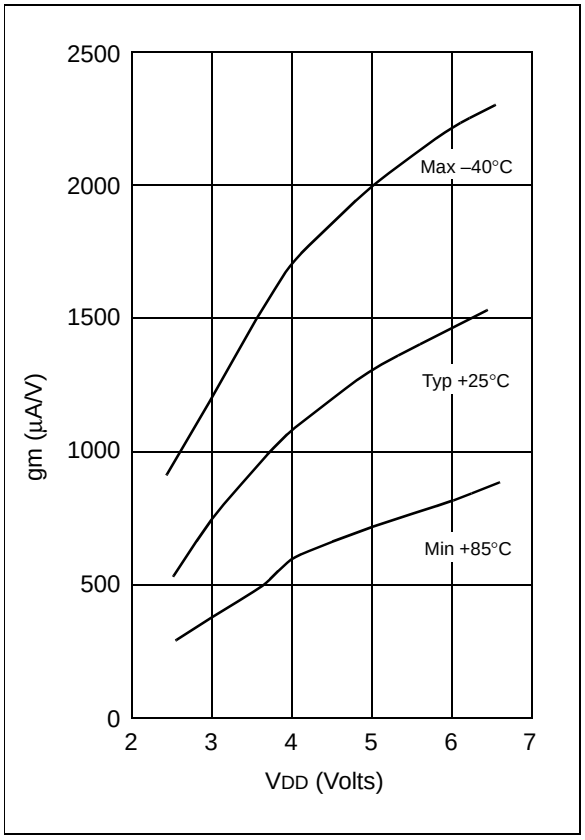

FIGURE 11-20: IOH vs. VOH, VDD = 5 V

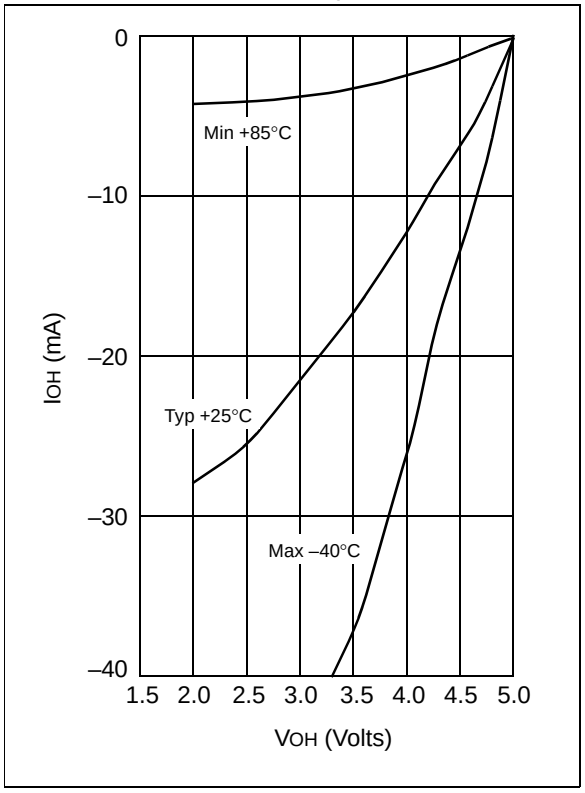

FIGURE 11-21: IOL vs. VOL, VDD = 3 V

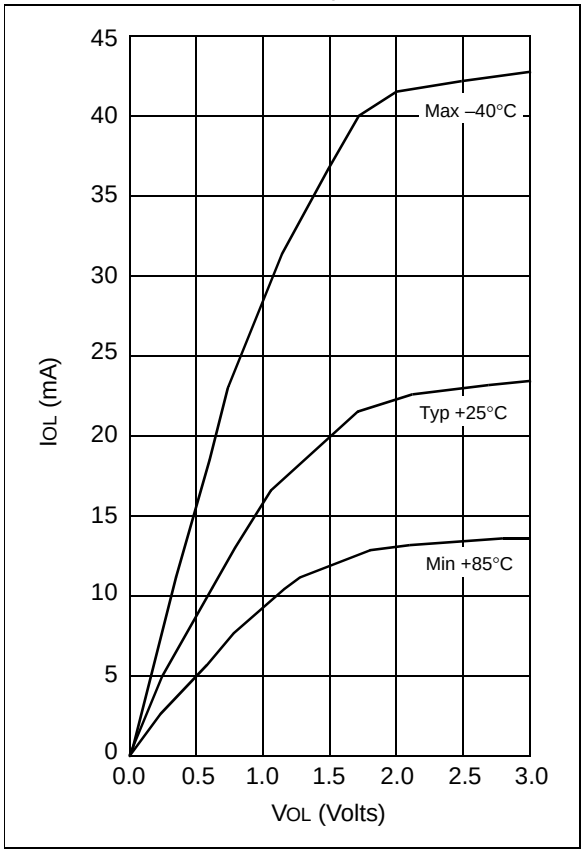

FIGURE 11-22: IOL vs. VOL, VDD = 5 V

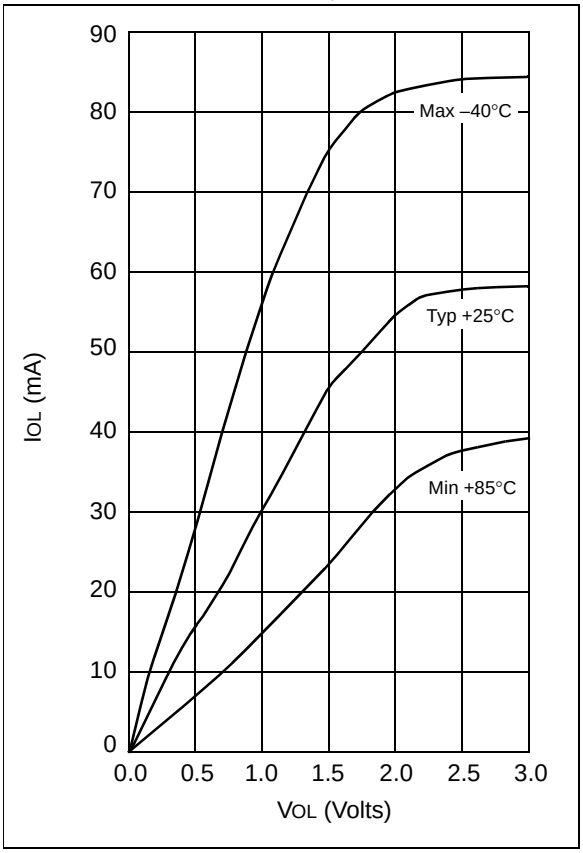

TABLE 11-2: INPUT CAPACITANCE FOR PIC16C54/56

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

TABLE 11-3: INPUT CAPACITANCE FOR PIC16C55/57

Pin	Typical Capacitance (pF)	
	28L PDIP (600 mil)	28L SOIC
RA port	5.2	4.8
RB port	5.6	4.7
RC port	5.0	4.1
$\overline{\text{MCLR}}$	17.0	17.0
OSC1	6.6	3.5
OSC2/CLKOUT	4.6	3.5
T0CKI	4.5	3.5

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

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12.0 ELECTRICAL CHARACTERISTICS - PIC16CR54A

Absolute Maximum Ratings†

Ambient Temperature under bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V

Voltage on $\overline{MCLR}$ with respect to V_{SS} **(2)** ..... 0 to +14V

Voltage on all other pins with respect to V_{SS} ..... –0.6V to (V_{DD} + 0.6V)

Total Power Dissipation **(1)** ..... 800 mW

Max. Current out of V_{SS} pin ..... 150 mA

Max. Current into V_{DD} pin ..... 50 mA

Max. Current into an input pin (T0CKI only) ..... ±500 μA

Input Clamp Current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA

Output Clamp Current, I_{OK} (V_0 < 0 or V_0 > V_{DD}) ..... ±20 mA

Max. Output Current sunk by any I/O pin ..... 25 mA

Max. Output Current sourced by any I/O pin ..... 20 mA

Max. Output Current sourced by a single I/O port (PORTA or B) ..... 40 mA

Max. Output Current sunk by a single I/O port (PORTA or B) ..... 50 mA

Note 1: Power Dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

2: Voltage spikes below Vss at the $\overline{MCLR}$ pin, inducing currents greater than 80 mA may cause latch-up. Thus, a series resistor of 50 to 100Ω should be used when applying a low level to the $\overline{MCLR}$ pin rather than pulling this pin directly to Vss.

†NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

12.1 DC Characteristics: PIC16CR54A-04, 10, 20 (Commercial) PIC16CR54A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage RC and XT options HS option	VDD	 2.5 4.5		 6.25 5.5	 V V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) RC(4) and XT options HS option	IDD	 	 2.0 0.8 90 4.8 9.0	 3.6 1.8 350 10 20	 mA mA µA mA mA	 FOSC = 4.0 MHz, VDD = 6.0V FOSC = 4.0 MHz, VDD = 3.0V FOSC = 200 kHz, VDD = 2.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 20 MHz, VDD = 5.5V
Power-down Current(5) Commercial	IPD	 	 1.0 2.0 3.0 5.0	 6.0 8.0* 15 25	 µA µA µA µA	 VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled
Power-down Current(5) Industrial	IPD	 	 1.0 2.0 3.0 3.0 5.0	 8.0 10* 20* 18 45	 µA µA µA µA µA	 VDD = 2.5V, WDT disabled VDD = 4.0V, WDT disabled VDD = 4.0V, WDT enabled VDD = 6.0V, WDT disabled VDD = 6.0V, WDT enabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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12.2 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (extended)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage RC, XT and LP options HS options	VDD	 3.25 4.5	 — —	 6.0 5.5	 V V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3) RC(4) and XT options HS option	IDD	 — — —	 1.8 4.8 9.0	 3.3 10 20	 mA mA mA	 FOSC = 4.0 MHz, VDD = 5.5V FOSC = 10 MHz, VDD = 5.5V FOSC = 16 MHz, VDD = 5.5V
Power-down Current(5)	IPD	 — —	 5.0 0.8	 22 18	 µA µA	 VDD = 3.25V, WDT enabled VDD = 3.25V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

12.3 DC Characteristics: PIC16LCR54A-04 (Commercial) PIC16LCR54A-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD	2.0	—	6.25	V	LP Option
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD Start Voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD Rise Rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD	—	10	20	µA	FOSC = 32 kHz, VDD = 2.0V
				70	µA	FOSC = 32 kHz, VDD = 6.0V
Power-down Current(5) Commercial	IPD	—	1.0	6.0	µA	VDD = 2.5V, WDT disabled
		—	2.0	8.0*	µA	VDD = 4.0V, WDT disabled
		—	3.0	15	µA	VDD = 6.0V, WDT disabled
		—	5.0	25	µA	VDD = 6.0V, WDT enabled
Power-down Current(5) Industrial	IPD	—	1.0	8.0	µA	VDD = 2.5V, WDT disabled
		—	2.0	10*	µA	VDD = 4.0V, WDT disabled
		—	3.0	20*	µA	VDD = 4.0V, WDT enabled
		—	3.0	18	µA	VDD = 6.0V, WDT disabled
		—	5.0	45	µA	VDD = 6.0V, WDT enabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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12.4 DC Characteristics: PIC16CR54A-04, 10, 20, PIC16LCR54A-04 (Commercial) PIC16CR54A-04I, 10I, 20I, PIC16LCR54A-04I (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 12.1 and Section 12.3.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS	—	0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS	—	0.15 VDD	V	RC option only(4)
OSC1		VSS	—	0.15 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		2.0	—	VDD	V	VDD = 3.0V to 5.5V(5)
		0.6 VDD	—	VDD	V	Full VDD range(5)
MCLR (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.85 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1.0		+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5.0			µA	VPIN = VSS + 0.25V(2)
			0.5	+5.0	µA	VPIN = VDD(2)
T0CKI		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.5	V	IOL = 10 mA, VDD = 6.0V
OSC2/CLKOUT		—	—	0.5	V	IOL = 1.9 mA, VDD = 6.0V, RC option only
Output High Voltage(3)	VOH					
I/O ports		VDD –0.5	—	—	V	IOH = –4.0 mA, VDD = 6.0V
OSC2/CLKOUT		VDD –0.5	—	—	V	IOH = –0.8 mA, VDD = 6.0V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

12.5 DC Characteristics: PIC16CR54A-04E, 10E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C Operating Voltage VDD range is described in Section 12.2.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		Vss	—	0.15 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		Vss	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		Vss	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		Vss	—	0.15 VDD	V	RC option only(4)
OSC1		Vss	—	0.3 VDD	V	XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.45 VDD	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
		0.36 VDD	—	VDD	V	VDD > 5.5V
MCLR (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		–1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
MCLR		–5.0			µA	VPIN = VSS + 0.25V(2)
			0.5	+5.0	µA	VPIN = VDD(2)
T0CKI		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		–3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage (3)	VOH					
I/O ports		VDD –0.7	—	—	V	IOH = –5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD –0.7	—	—	V	IOH = –1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

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12.6 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

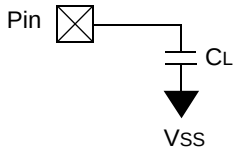
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 12-1: LOAD CONDITIONS



C_L = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

12.7 Timing Diagrams and Specifications

FIGURE 12-2: EXTERNAL CLOCK TIMING - PIC16CR54A

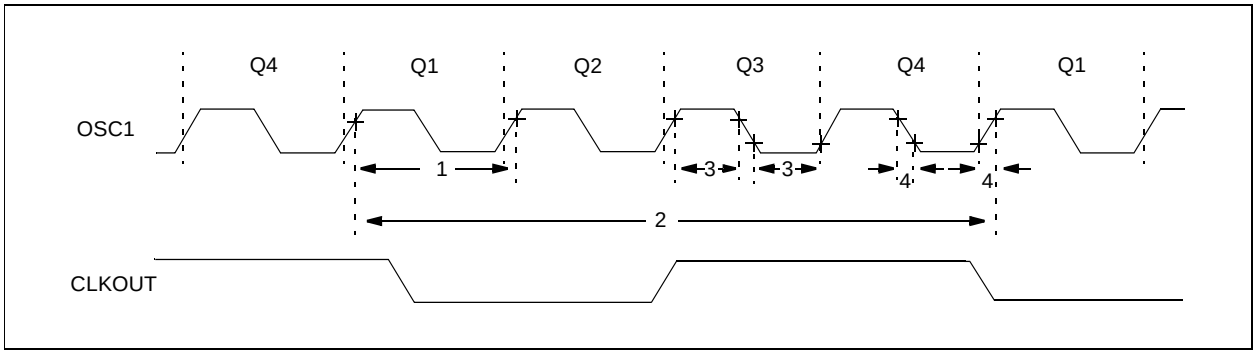


TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 12.1, Section 12.2 and Section 12.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			0.1	—	4.0	MHz	XT osc mode
			4.0	—	4.0	MHz	HS osc mode (04)
			4.0	—	10	MHz	HS osc mode (10)
			4.0	—	20	MHz	HS osc mode (20)
			5.0	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16CR54A (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 12.1, Section 12.2 and Section 12.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	10,000	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

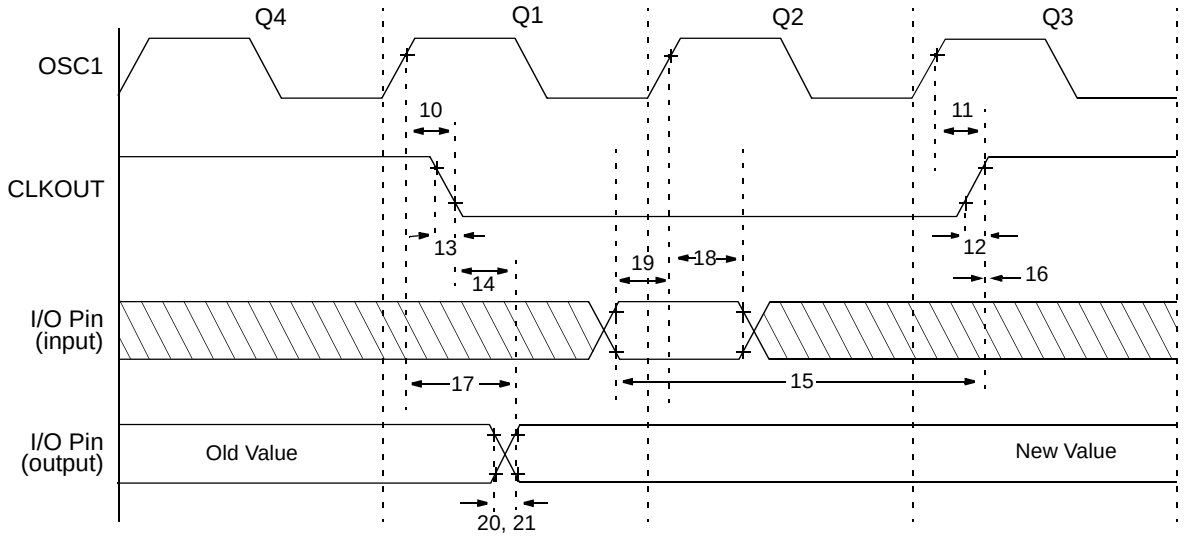
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 12-3: CLKOUT AND I/O TIMING - PIC16CR54A



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 12-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16CR54A

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 12.1, Section 12.2 and Section 12.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 12-1 for loading conditions.

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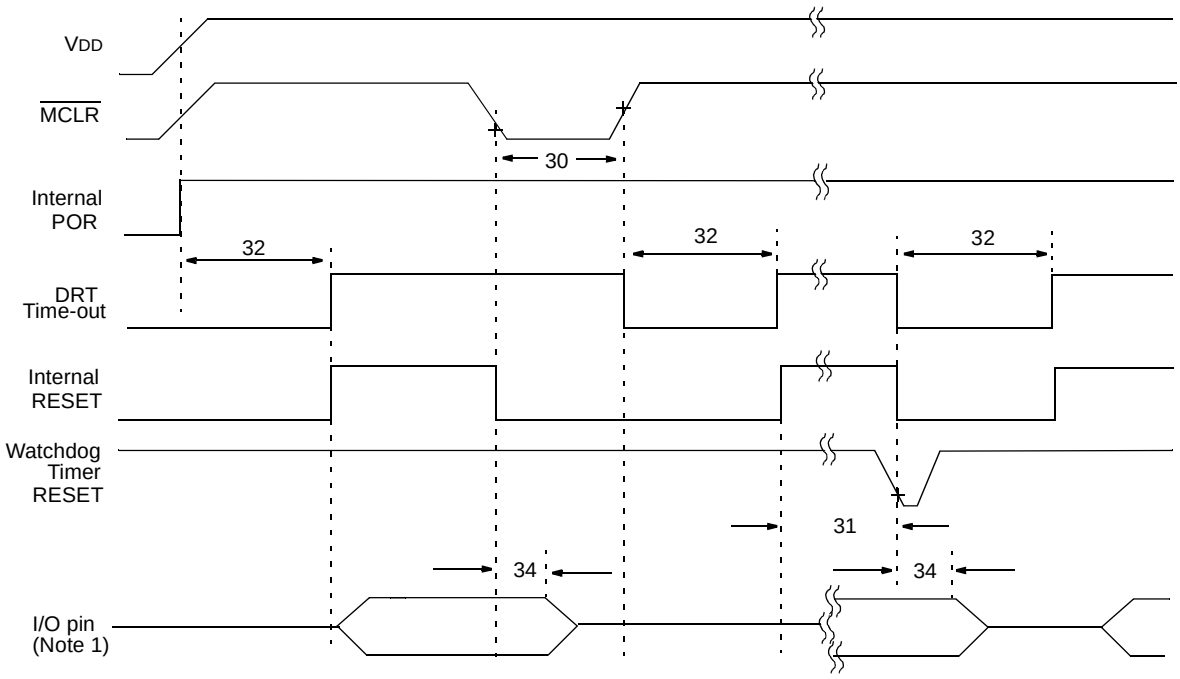
FIGURE 12-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16CR54A



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 12-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16CR54A

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 12.1, Section 12.2 and Section 12.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	1.0*	—	—	µs	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	7.0*	18*	40*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	7.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	—	—	1.0*	µs	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-5: TIMER0 CLOCK TIMINGS - PIC16CR54A

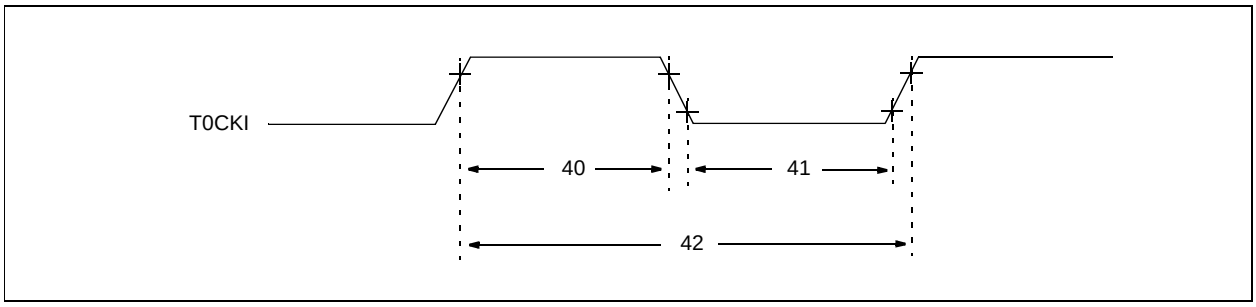


TABLE 12-4: TIMER0 CLOCK REQUIREMENTS - PIC16CR54A

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 12.1, Section 12.2 and Section 12.3.				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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13.0 ELECTRICAL CHARACTERISTICS - PIC16C54A

Absolute Maximum Ratings†

Ambient temperature under bias ..... –55°C to +125°C
Storage temperature ..... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... 0 to +14V
Voltage on all other pins with respect to V_{SS} ..... –0.6V to (V_{DD} + 0.6V)
Total power dissipation(1) ..... 800 mW
Max. current out of V_{SS} pin ..... 150 mA
Max. current into V_{DD} pin ..... 100 mA
Max. current into an input pin (T0CKI only) ..... ±500 µA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. output current sunk by any I/O pin ..... 25 mA
Max. output current sourced by any I/O pin ..... 20 mA
Max. output current sourced by a single I/O port (PORTA or B) ..... 50 mA
Max. output current sunk by a single I/O port (PORTA or B) ..... 50 mA

Note 1: Power dissipation is calculated as follows: $Pdis = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

13.1 DC Characteristics: PIC16C54A-04, 10, 20 (Commercial) PIC16C54A-04I, 10I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT, RC and LP options		3.0	—	6.25	V	
HS option		4.5	—	5.5	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
XT and RC(4) options		—	1.8	2.4	mA	FOSC = 4.0 MHz, VDD = 5.5V
HS option		—	2.4	8.0	mA	FOSC = 10 MHz, VDD = 5.5V
		—	4.5	16	mA	FOSC = 20 MHz, VDD = 5.5V
LP option, Commercial		—	14	29	µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
LP option, Industrial		—	17	37	µA	FOSC = 32 kHz, VDD = 3.0V, WDT disabled
Power-down Current(5)	IPD					
Commercial		—	4.0	12	µA	VDD = 3.0V, WDT enabled
		—	0.25	4.0	µA	VDD = 3.0V, WDT disabled
Industrial		—	5.0	14	µA	VDD = 3.0V, WDT enabled
		—	0.3	5.0	µA	VDD = 3.0V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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13.2 DC Characteristics: PIC16C54A-04E, 10E, 20E (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (extended)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT and RC options		3.5	—	5.5	V	
HS option		4.5	—	5.5	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
XT and RC(4) options		—	1.8	3.3	mA	FOSC = 4.0 MHz, VDD = 5.5V
HS option		—	4.8	10	mA	FOSC = 10 MHz, VDD = 5.5V
		—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
Power-down Current(5)	IPD					
XT and RC options		—	5.0	22	µA	VDD = 3.5V, WDT enabled
		—	0.8	18	µA	VDD = 3.5V, WDT disabled
HS option		—	4.0	22	µA	VDD = 3.5V, WDT enabled
		—	0.25	18	µA	VDD = 3.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

13.3 DC Characteristics: PIC16LC54A-04 (Commercial) PIC16LC54A-04I (Industrial))

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT and RC options		3.0	—	6.25	V	
LP options		2.5	—	6.25	V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
XT and RC(4) options		—	0.5	2.5	mA	FOSC = 4.0 MHz, VDD = 5.5V
LP option, Commercial		—	11	27	µA	FOSC = 32 kHz, VDD = 2.5V WDT disabled
LP option, Industrial		—	11	35	µA	FOSC = 32 kHz, VDD = 2.5V WDT disabled
LP option, Extended		—	11	37	µA	FOSC = 32 kHz, VDD = 2.5V WDT disabled
Power-down Current(5)	IPD					
Commercial		—	2.5	12	µA	VDD = 2.5V, WDT enabled
		—	0.25	4.0	µA	VDD = 2.5V, WDT disabled
Industrial		—	2.5	14	µA	VDD = 2.5V, WDT enabled
		—	0.25	5.0	µA	VDD = 2.5V, WDT disabled
Extended		—	2.5	15	µA	VDD = 2.5V, WDT enabled
		—	0.25	7.0	µA	VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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13.4 DC Characteristics: PIC16C54A-04, 10, 20, PIC16LC54A-04, PIC16LV54A-02 (Commercial) PIC16C54A-04I, 10I, 20I, PIC16LC54A-04I, PIC16LV54A-02I (Industrial) PIC16C54A-04E, 10E, 20E (Extended)

DC Characteristics All Pins Except Power Supply Pins		**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –20°C ≤ TA ≤ +85°C (industrial - PIC16LV54A-02I) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O ports		VSS	—	0.2 VDD	V	Pin at hi-impedance
MCLR (Schmitt Trigger)		VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS	—	0.15 VDD	V	RC option only(4)
OSC1		VSS	—	0.3 VDD		XT, HS and LP options
Input High Voltage	VIH					
I/O ports		0.2 VDD+1V	—	VDD	V	For all VDD(5)
		2.0	—	VDD	V	4.0V < VDD ≤ 5.5V(5)
MCLR (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		-1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD,
		—	—	—	—	Pin at hi-impedance
MCLR		-5.0	—	+5.0	µA	VPIN = VSS +0.25V(2)
			0.5	+3.0	µA	VPIN = VDD(2)
T0CKI		-3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3.0	0.5	—	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage	VOH					
I/O ports(3)		VDD-0.7	—	—	V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD-0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the MCLR/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

5: The user may use the better of the two specifications.

13.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

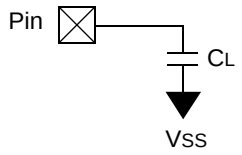
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 13-1: LOAD CONDITIONS - PIC16C54A



C_L = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

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13.6 Timing Diagrams and Specifications

FIGURE 13-2: EXTERNAL CLOCK TIMING - PIC16C54A

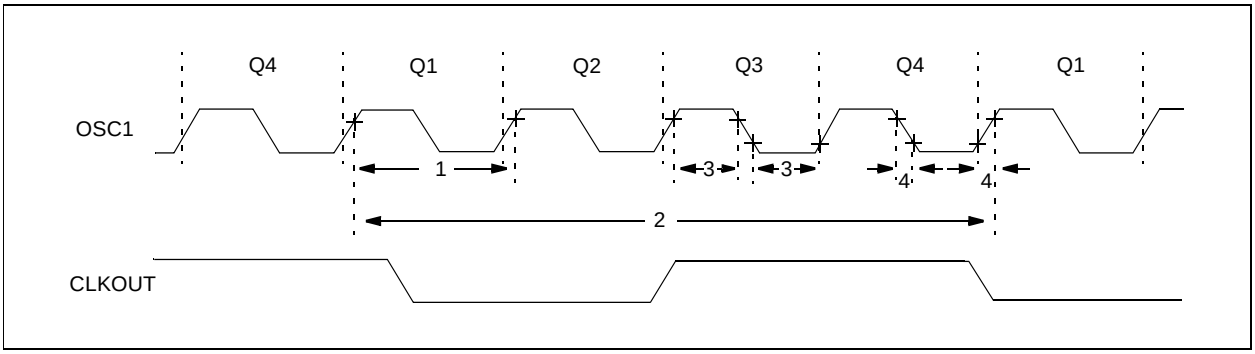

TABLE 13-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –20°C ≤ TA ≤ +85°C (industrial - PIC16LV54A-02I) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	XT osc mode
			DC	—	2.0	MHz	XT osc mode (PIC16LV54A)
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	10	MHz	HS osc mode (10)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			DC	—	2.0	MHz	RC osc mode (PIC16LV54A)
			0.1	—	4.0	MHz	XT osc mode
			0.1	—	2.0	MHz	XT osc mode (PIC16LV54A)
			4	—	4.0	MHz	HS osc mode (04)
			4	—	10	MHz	HS osc mode (10)
			4	—	20	MHz	HS osc mode (20)
			5	—	200	kHz	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the “max” cycle time limit is “DC” (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

TABLE 13-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C54A (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –20°C ≤ TA ≤ +85°C (industrial - PIC16LV54A-02I) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			500	—	—	ns	XT osc mode (PIC16LV54A)
			250	—	—	ns	HS osc mode (04)
			100	—	—	ns	HS osc mode (10)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			500	—	—	ns	RC osc mode (PIC16LV54A)
			250	—	10,000	ns	XT osc mode
			500	—	—	ns	XT osc mode (PIC16LV54A)
			250	—	250	ns	HS osc mode (04)
			100	—	250	ns	HS osc mode (10)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	85*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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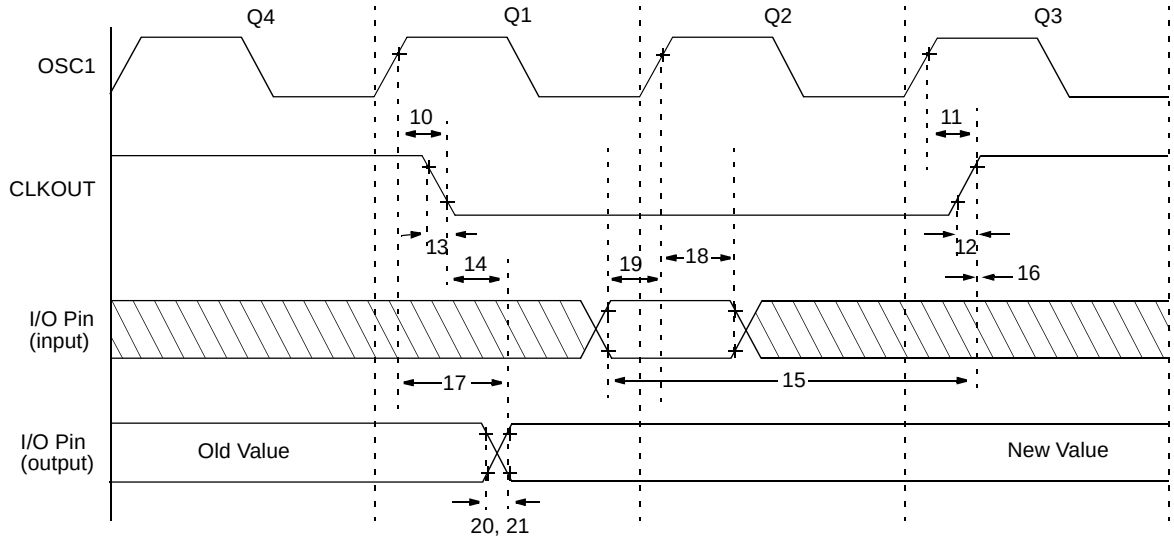
FIGURE 13-3: CLKOUT AND I/O TIMING - PIC16C54A



Note: All tests must be done with specified capacitive loads (see data sheet) 50 pF on I/O pins and CLKOUT.

TABLE 13-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C54A

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –20°C ≤ TA ≤ +85°C (industrial - PIC16LV54A-02I) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

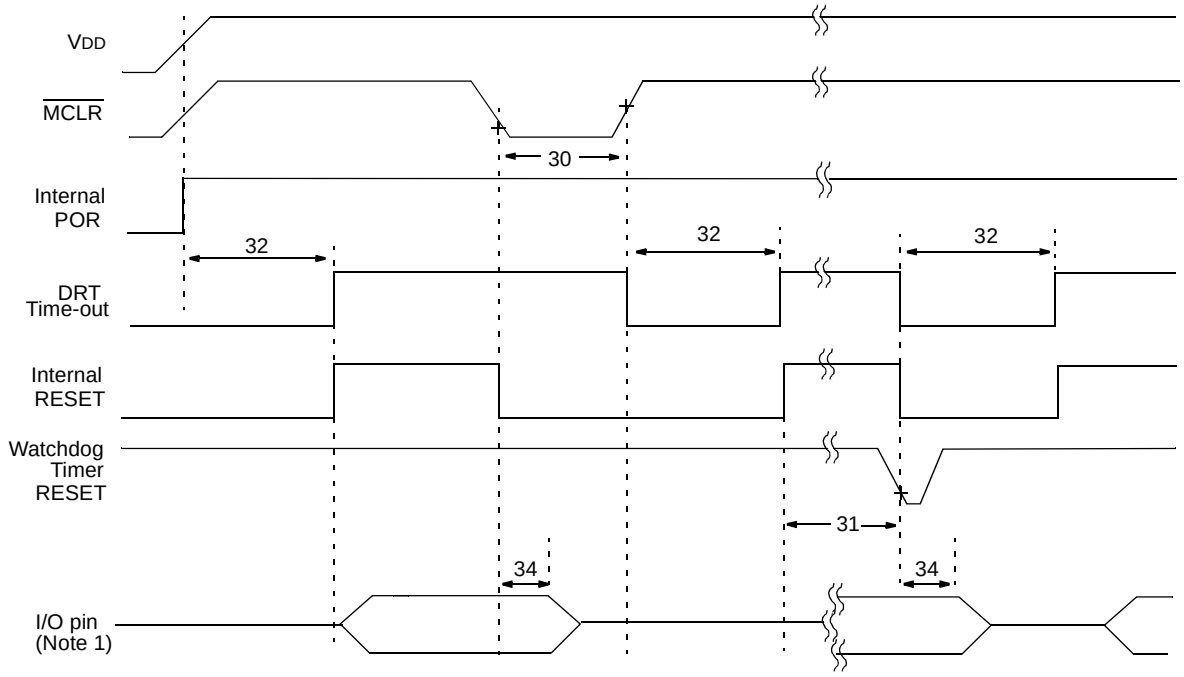
** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 14-1 for loading conditions.

FIGURE 13-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C54A



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 13-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C54A

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –20°C ≤ TA ≤ +85°C (industrial - PIC16LV54A-02I) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.					

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
30	TmcL	$\overline{MCLR}$ Pulse Width (low)	100* 1µs	— —	— —	ns —	VDD = 5.0V VDD = 5.0V (PIC16LV54A only)
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{MCLR}$ Low	— —	— —	100* 1µs	ns —	 (PIC16LV54A only)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 13-5: TIMER0 CLOCK TIMINGS - PIC16C54A

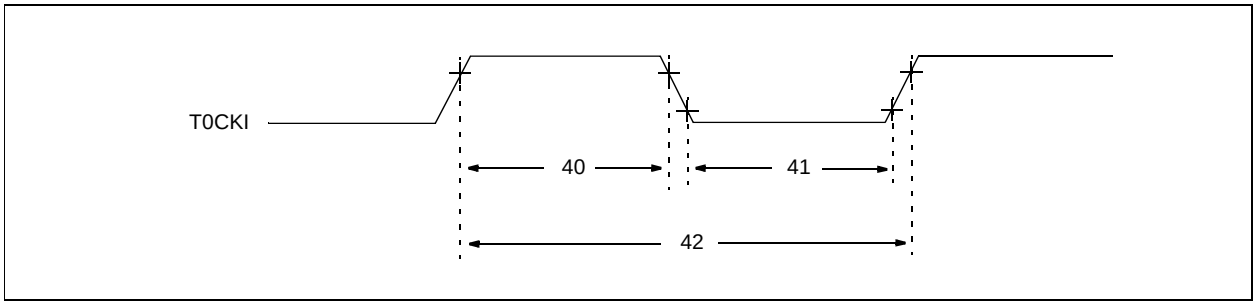

TABLE 13-4: TIMER0 CLOCK REQUIREMENTS - PIC16C54A

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –20°C ≤ TA ≤ +85°C (industrial - PIC16LV54A-02I) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 13.1, Section 13.2 and Section 13.3.

Param No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

NOTES:

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14.0 DC AND AC CHARACTERISTICS - PIC16C54A

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution, while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 14-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

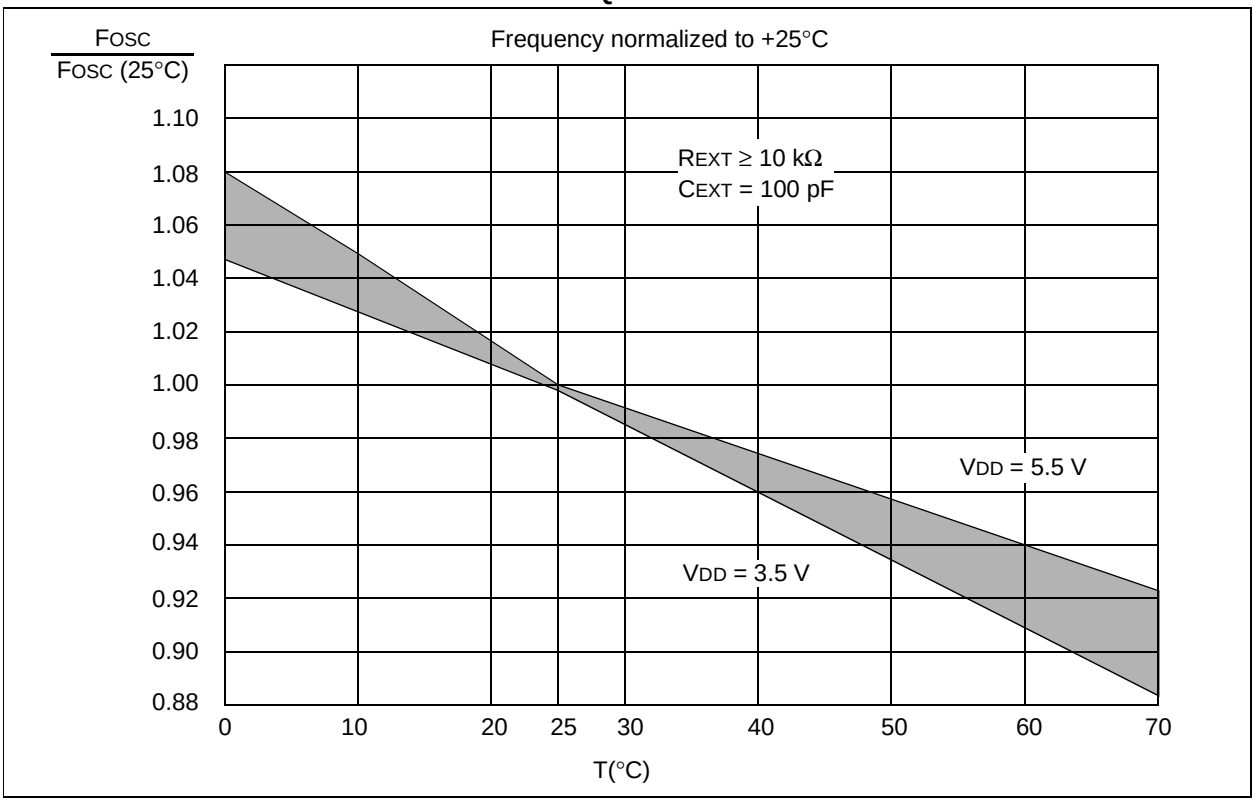

TABLE 14-1: RC OSCILLATOR FREQUENCIES

CEXT	REXT	Average Fosc @ 5 V, 25°C	
20 pF	3.3 k	4.973 MHz	± 27%
	5 k	3.82 MHz	± 21%
	10 k	2.22 MHz	± 21%
	100 k	262.15 kHz	± 31%
100 pF	3.3 k	1.63 MHz	± 13%
	5 k	1.19 MHz	± 13%
	10 k	684.64 kHz	± 18%
	100 k	71.56 kHz	± 25%
300 pF	3.3 k	660 kHz	± 10%
	5.0 k	484.1 kHz	± 14%
	10 k	267.63 kHz	± 15%
	160 k	29.44 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5 V.

FIGURE 14-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF

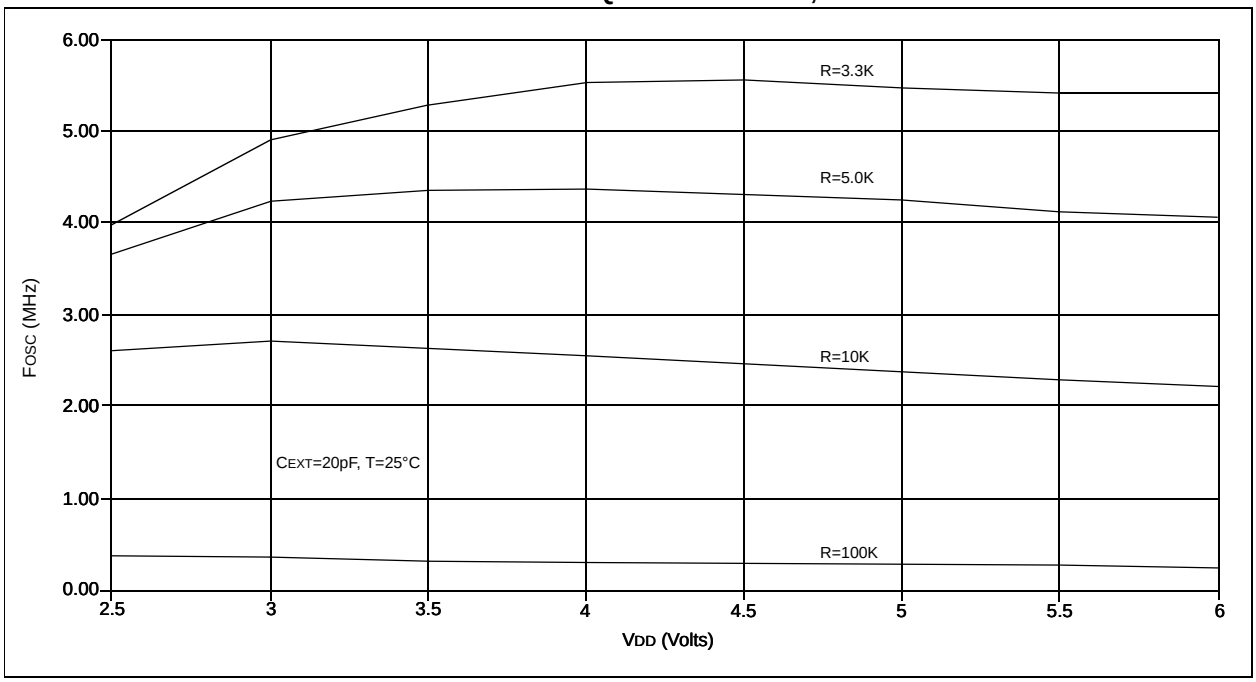

FIGURE 14-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF

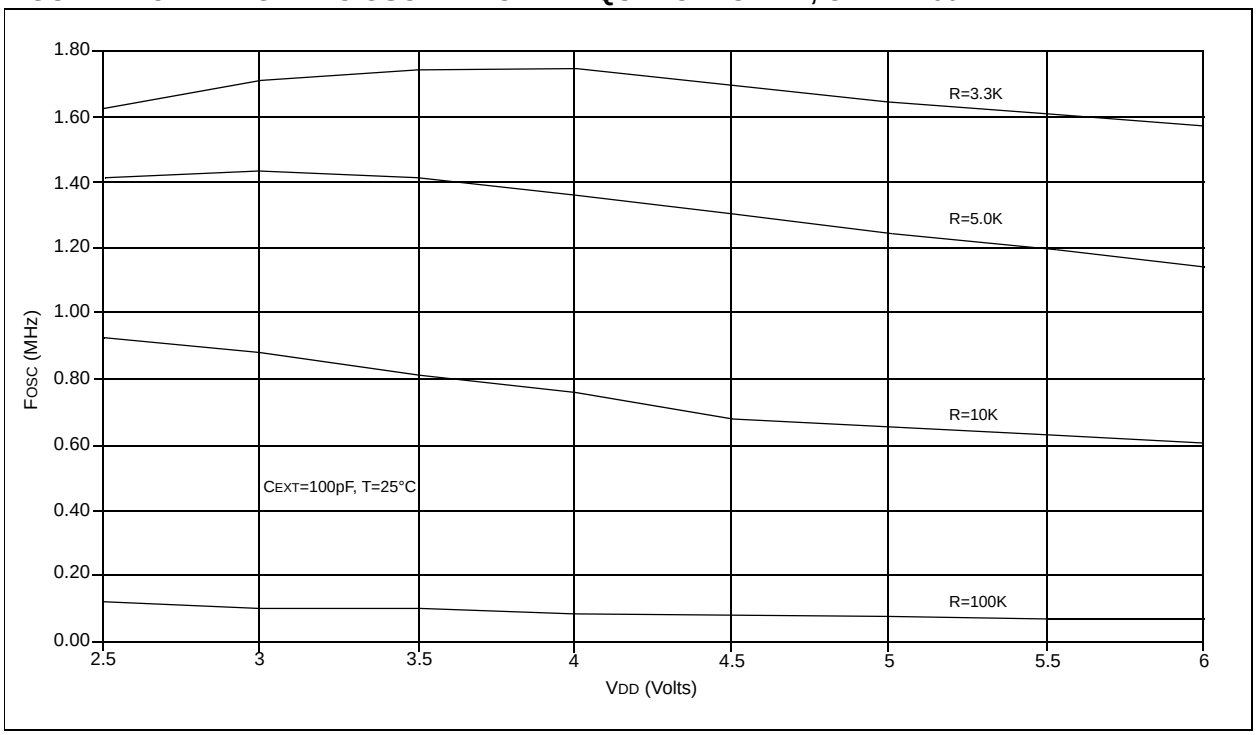

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FIGURE 14-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF

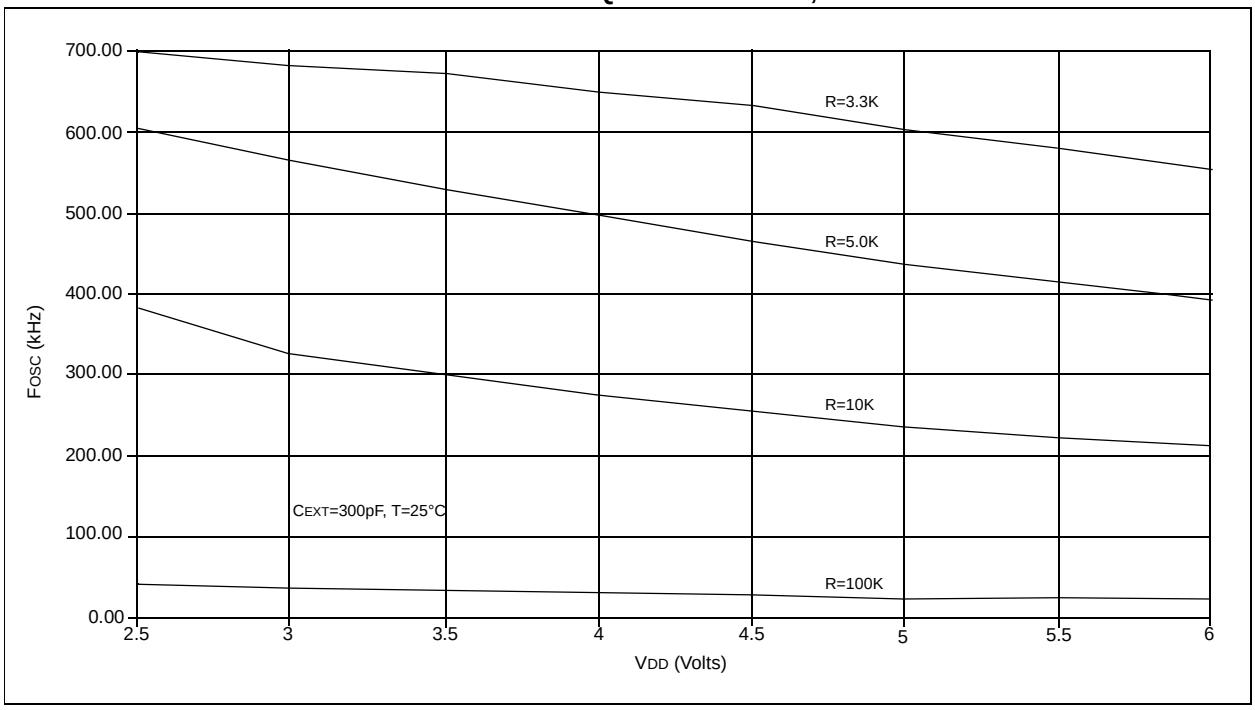


FIGURE 14-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)

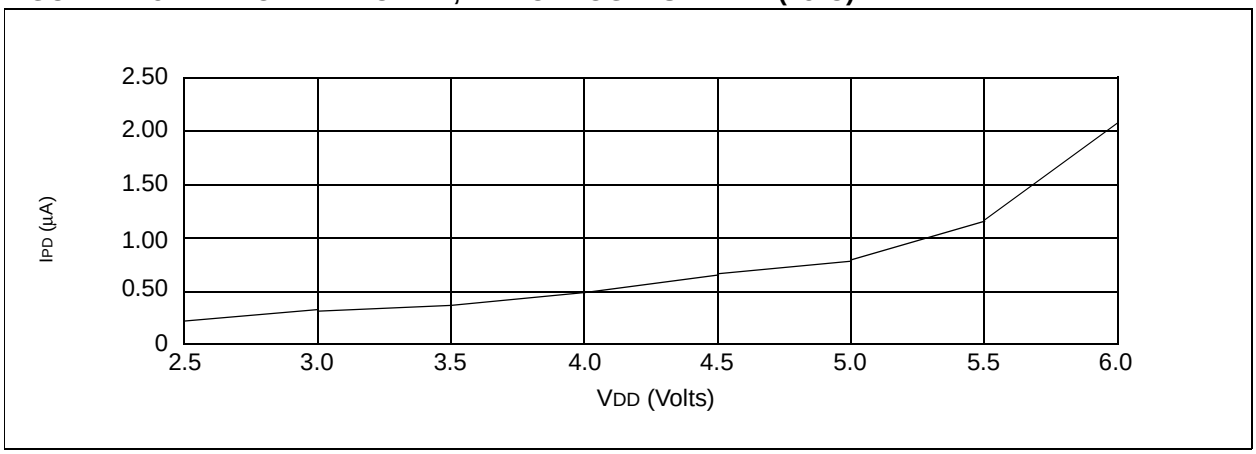


FIGURE 14-6: VTH (INPUT THRESHOLD VOLTAGE) OF I/O PINS vs. VDD

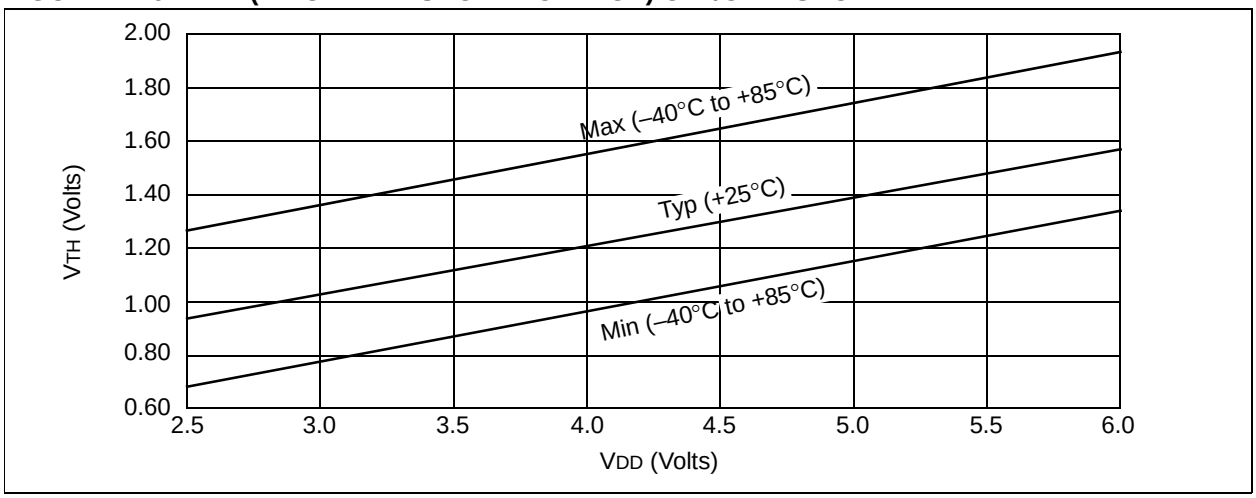
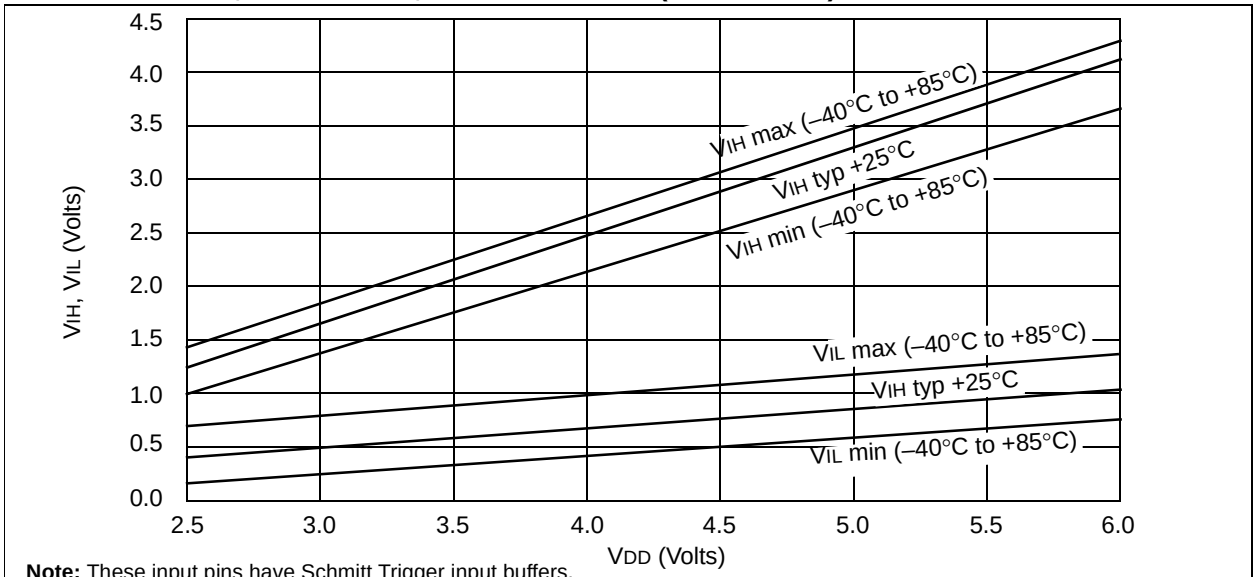


FIGURE 14-7: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (IN RC MODE) vs. VDD



Note: These input pins have Schmitt Trigger input buffers.

FIGURE 14-8: VTH (INPUT THRESHOLD VOLTAGE) OF OSC1 INPUT (IN XT, HS, AND LP MODES) vs. VDD

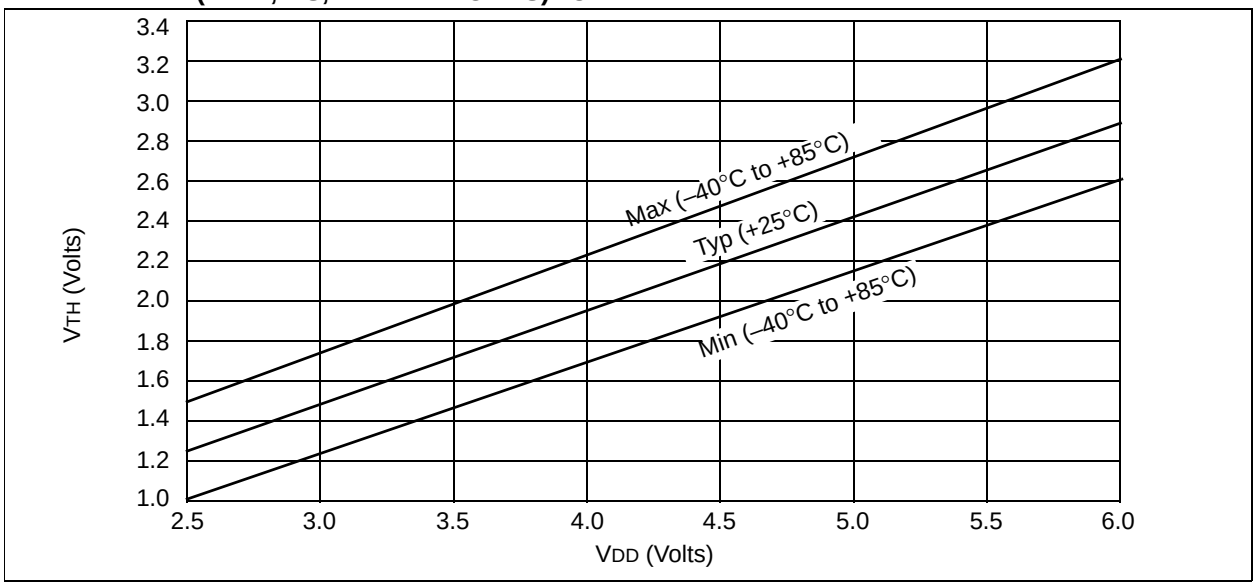


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FIGURE 14-9: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20 pF, 25°C)

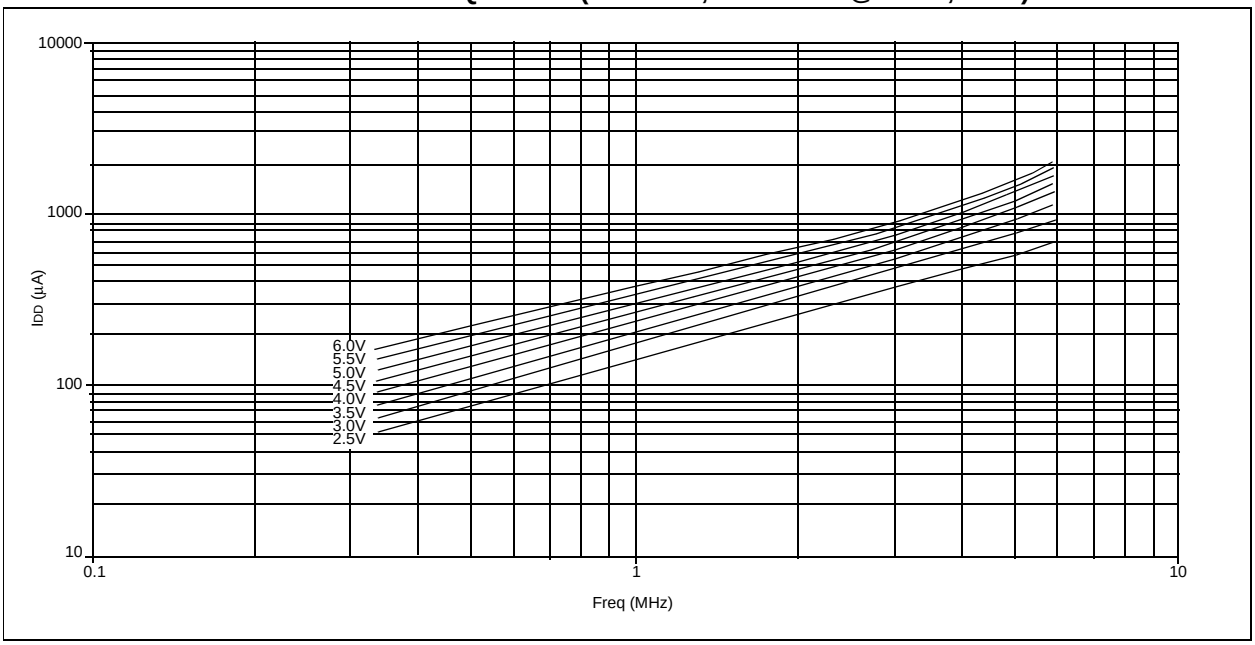

FIGURE 14-10: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20 pF, –40°C TO +85°C)

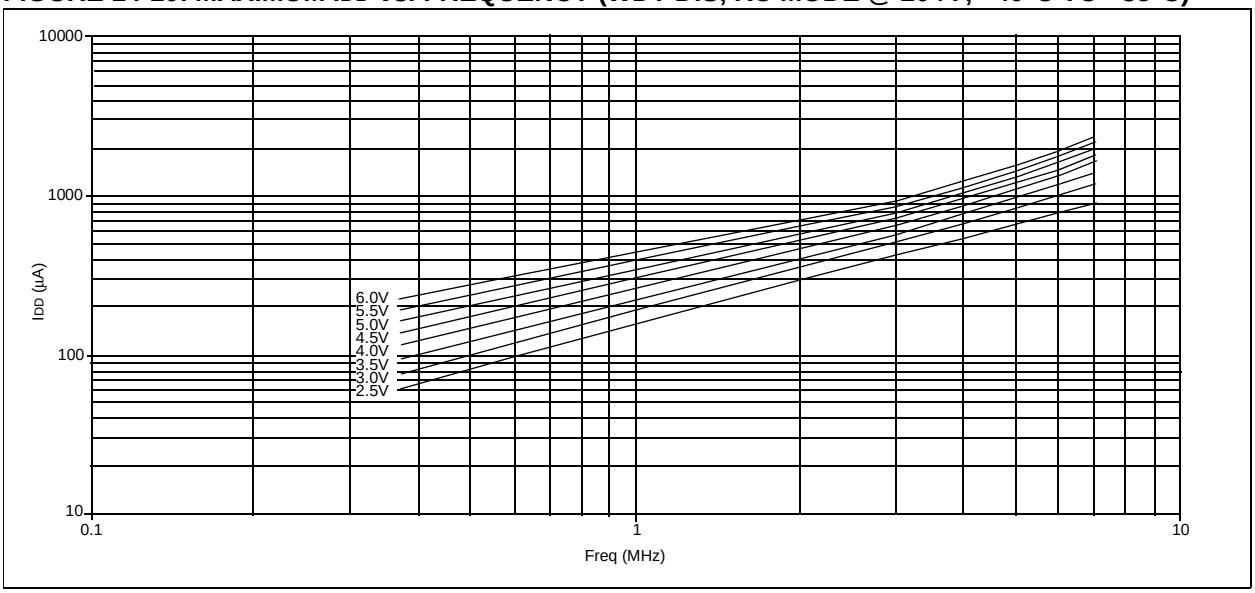

FIGURE 14-11: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 100 pF, 25°C)

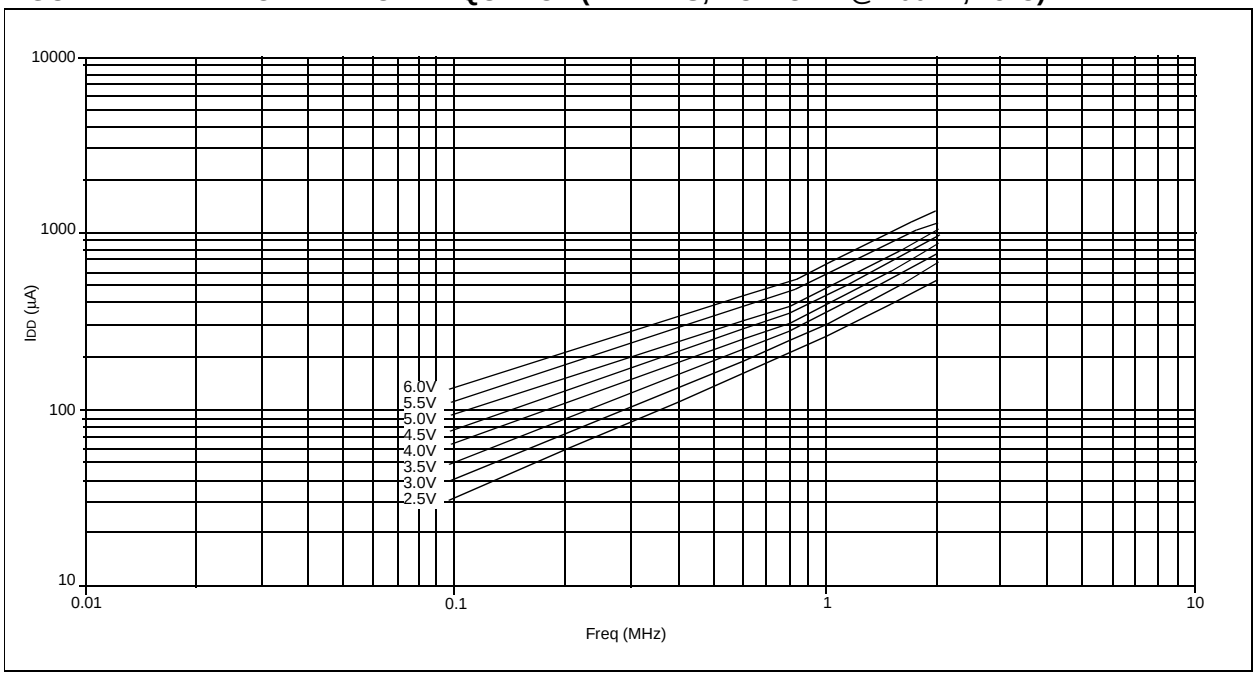

FIGURE 14-12: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 100 pF, –40°C TO +85°C)

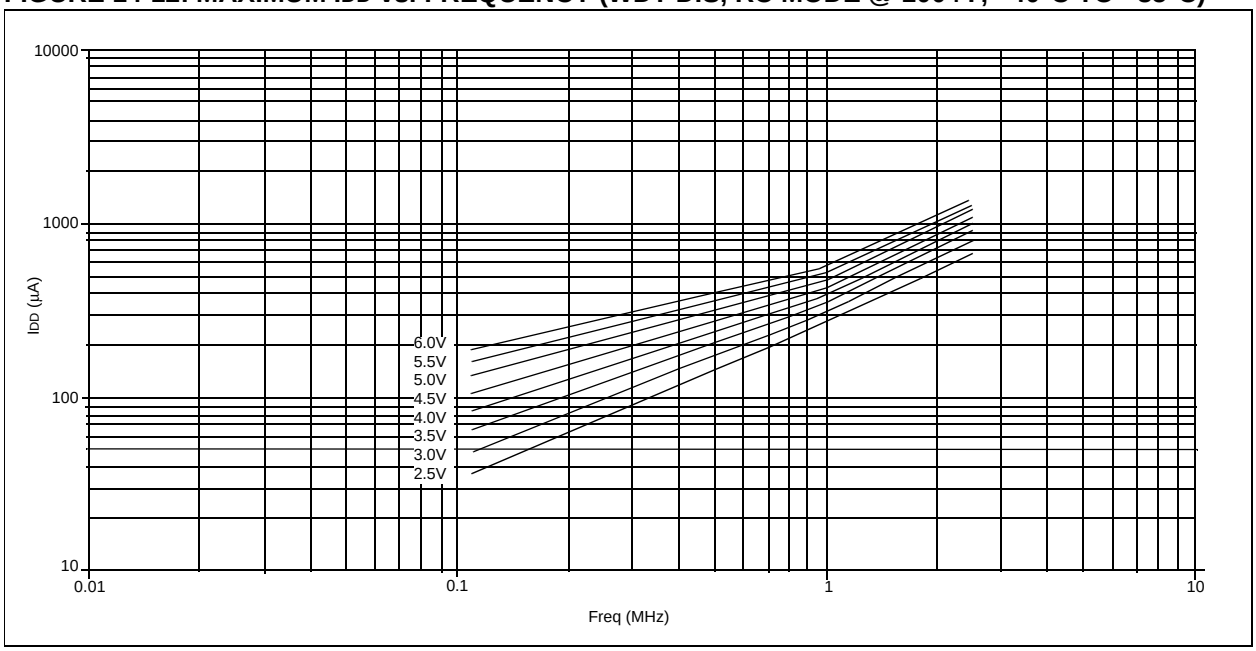

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FIGURE 14-13: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 300 pF, 25°C)

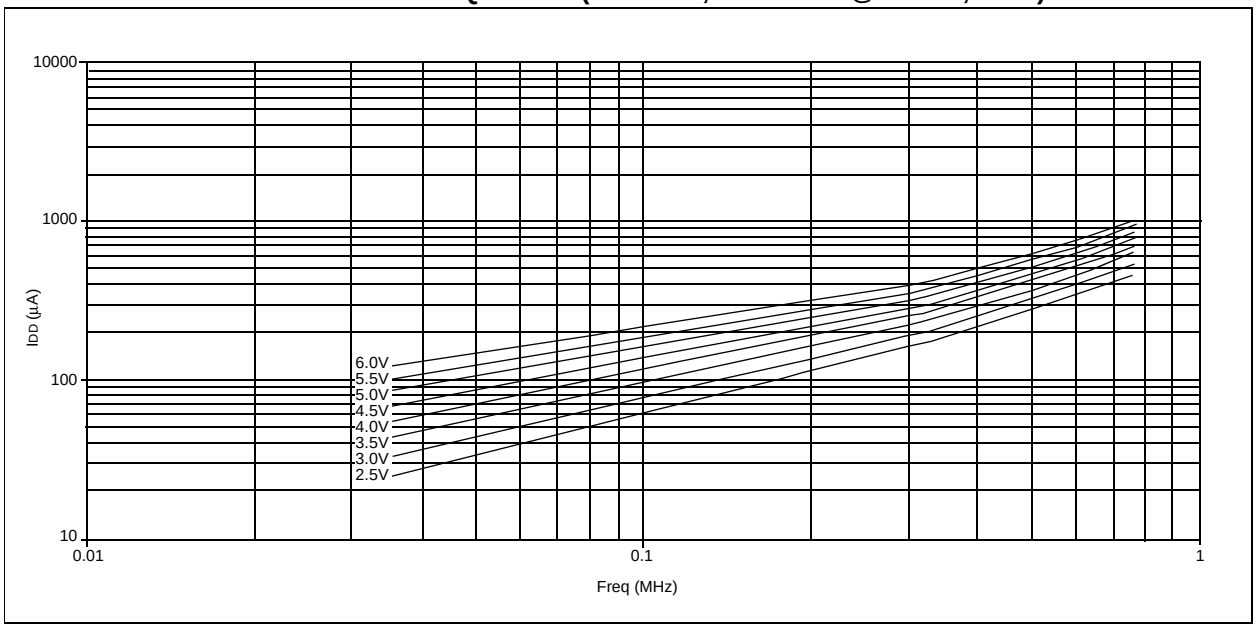

FIGURE 14-14: MAXIMUM IDD vs. FREQUENCY (WDT DIS, RC MODE @ 300 pF, –40°C TO +85°C)

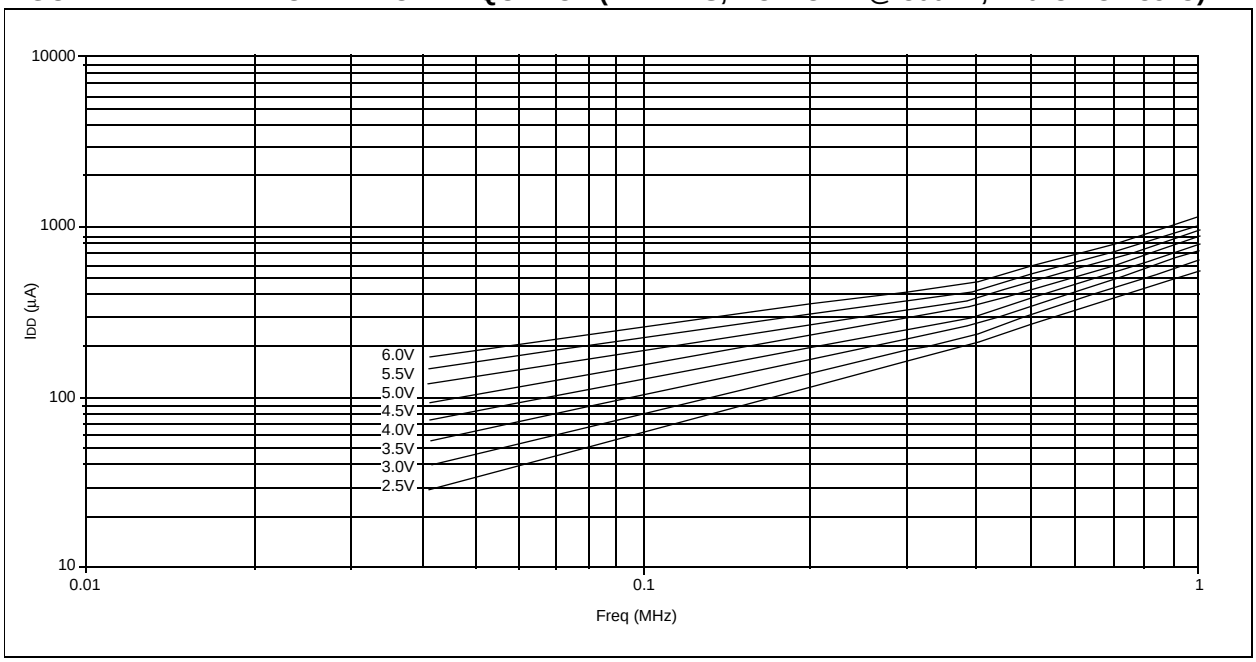

FIGURE 14-15: WDT TIMER TIME-OUT PERIOD vs. VDD

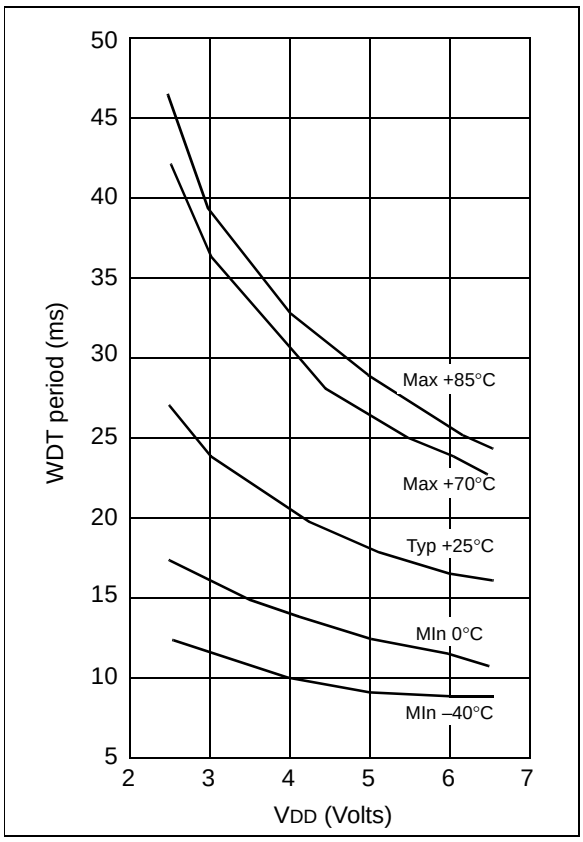

TABLE 14-2: INPUT CAPACITANCE FOR PIC16C54A/C58A

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

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FIGURE 14-16: TRANSCONDUCTANCE (gm) OF HS OSCILLATOR vs. VDD

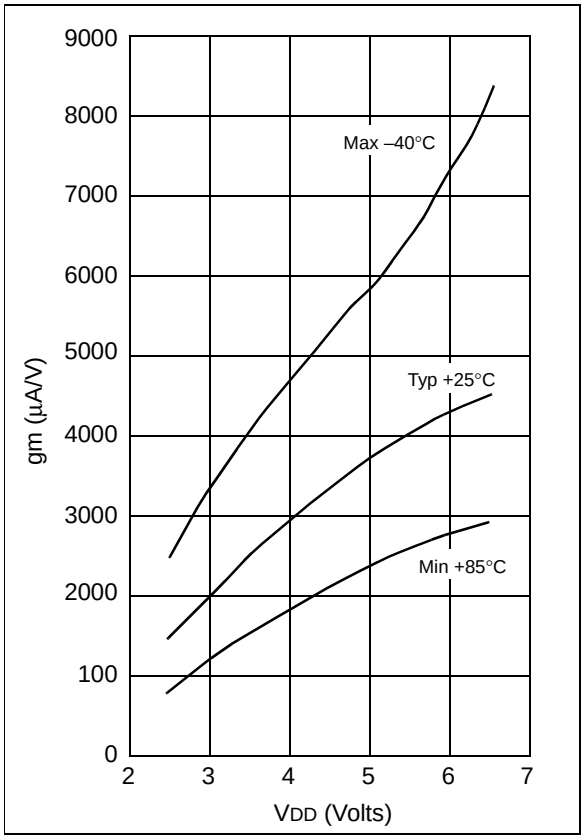


FIGURE 14-17: TRANSCONDUCTANCE (gm) OF LP OSCILLATOR vs. VDD

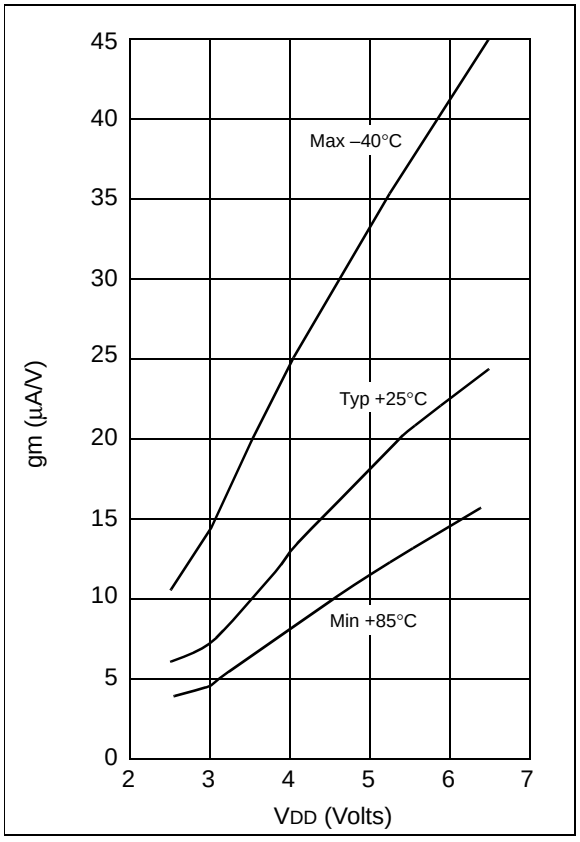


FIGURE 14-18: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

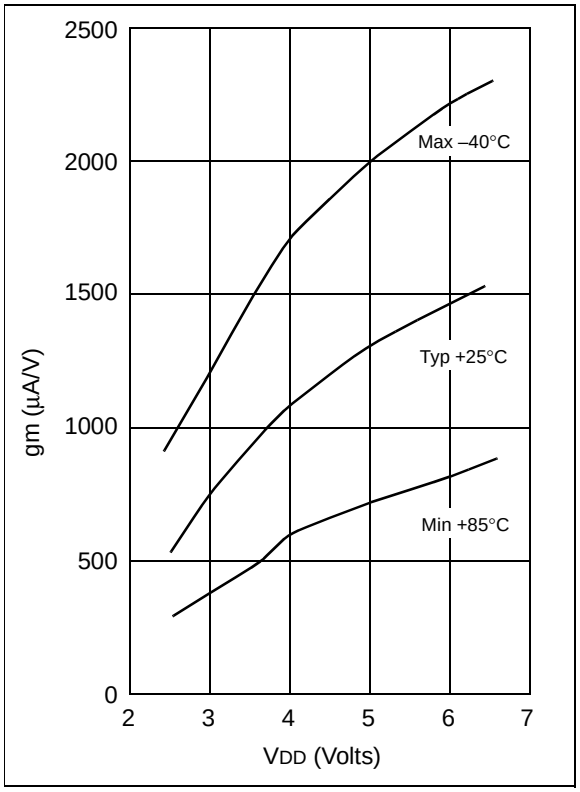


FIGURE 14-19: I_{OH} vs. V_{OH}, V_{DD} = 3 V

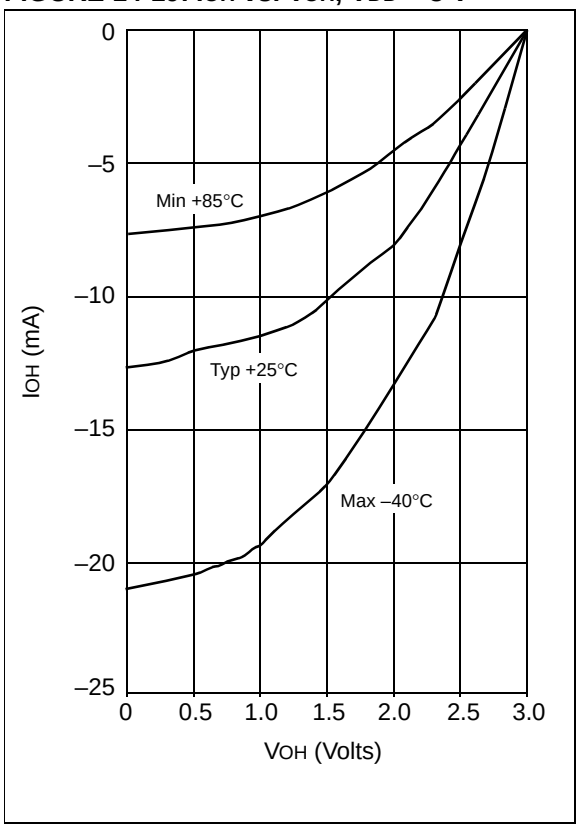


FIGURE 14-20: I_{OH} vs. V_{OH}, V_{DD} = 5 V

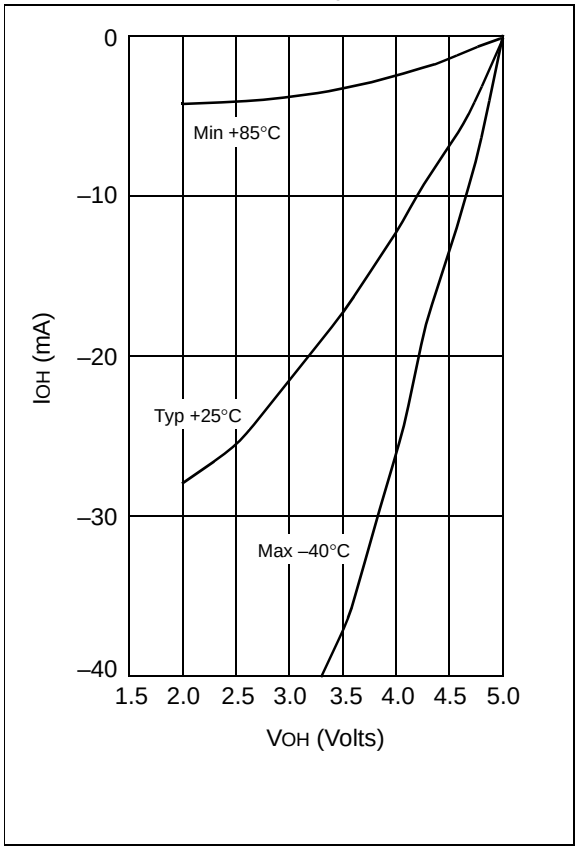


FIGURE 14-21: I_{OL} vs. V_{OL}, V_{DD} = 3 V

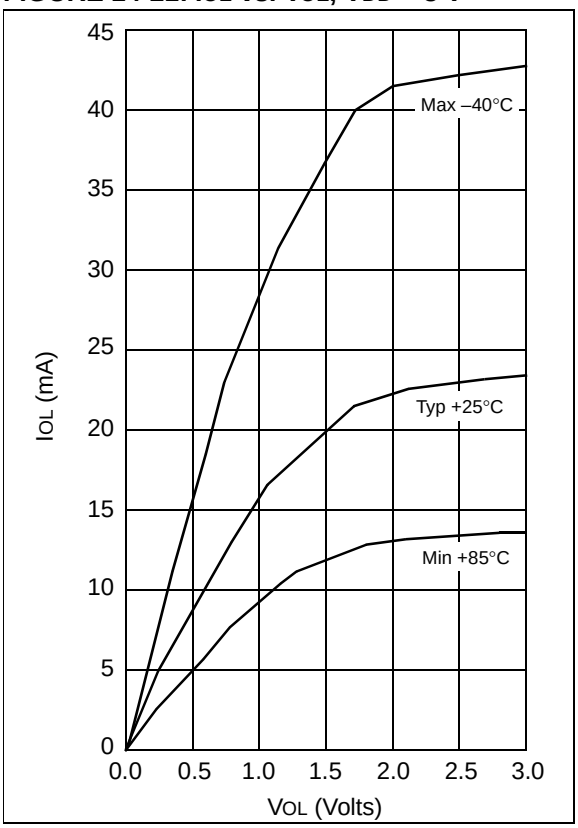
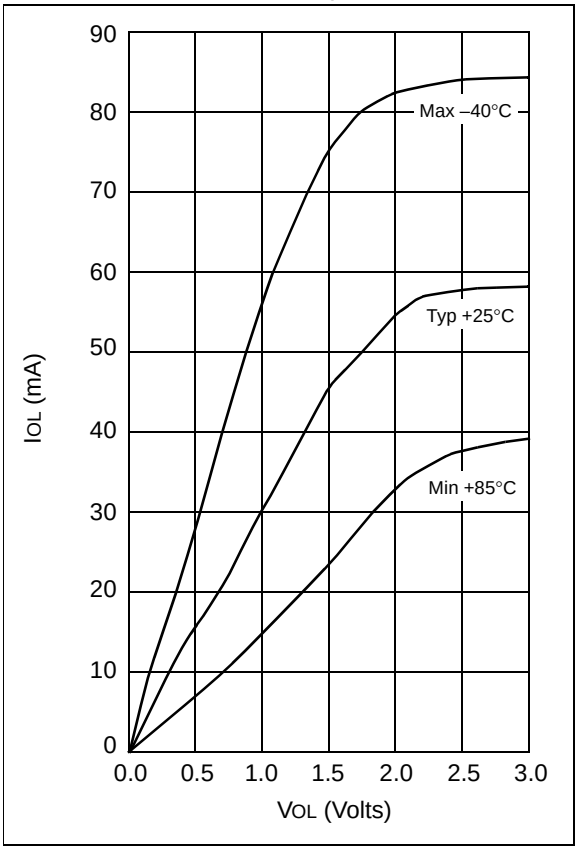


FIGURE 14-22: I_{OL} vs. V_{OL}, V_{DD} = 5 V



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15.0 ELECTRICAL CHARACTERISTICS - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B

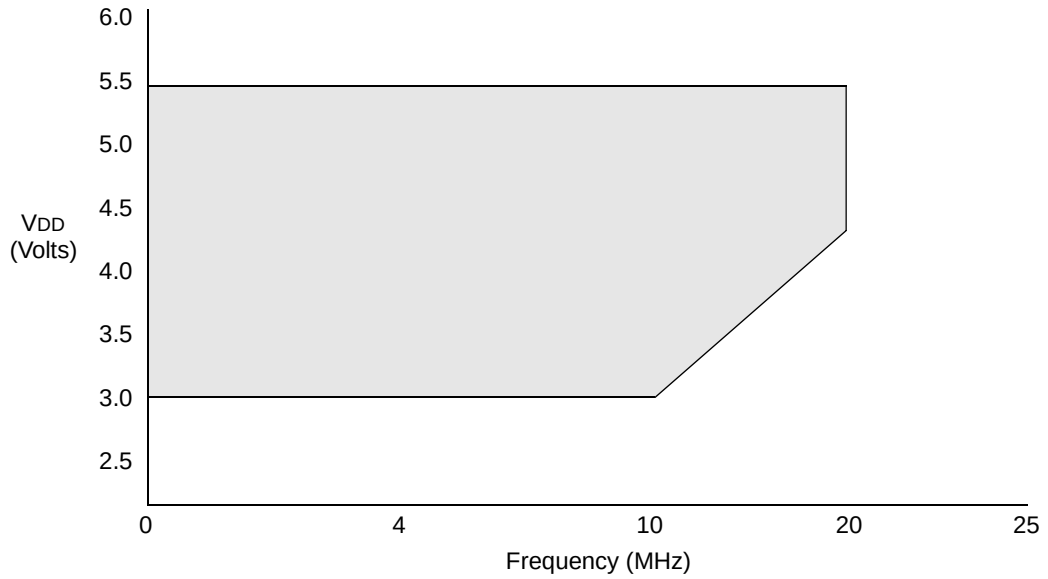
Absolute Maximum Ratings†

Ambient temperature under bias ..... –55°C to +125°C
Storage temperature ..... –65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... 0 to +7.5V
Voltage on $\overline{MCLR}$ with respect to V_{SS} ..... 0 to +14V
Voltage on all other pins with respect to V_{SS} ..... –0.6V to (V_{DD} + 0.6V)
Total power dissipation(1) ..... 800 mW
Max. current out of V_{SS} pin ..... 150 mA
Max. current into V_{DD} pin ..... 100 mA
Max. current into an input pin (T0CKI only) ..... ±500 µA
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DD}) ..... ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DD}) ..... ±20 mA
Max. output current sunk by any I/O pin ..... 25 mA
Max. output current sourced by any I/O pin ..... 20 mA
Max. output current sourced by a single I/O (Port A, B or C) ..... 50 mA
Max. output current sunk by a single I/O (Port A, B or C) ..... 50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum(V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

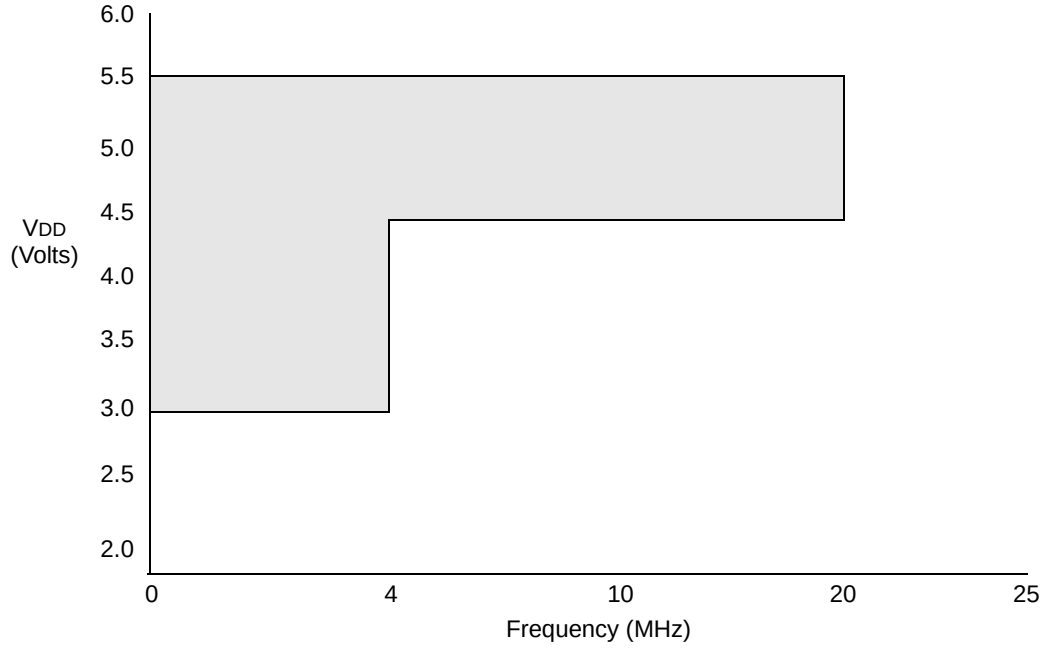
FIGURE 15-1: PIC16C54C VOLTAGE-FREQUENCY GRAPH, 0°C ≤ TA ≤ +70°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

FIGURE 15-2: PIC16C54C VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA < 0°C, +70°C < TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

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15.1 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial) PIC16C54C/C55A/C56A/C57C/C58B-04I, 20I (Industrial) PIC16CR54B/CR/54C/CR56A/CR57C/CR58B-04I, 20I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT, RC, LP and HS options		3.0	—	5.5	V	HS Option from 0 - 10MHz
HS option		4.5	—	5.5	V	HS Option from 0 - 20MHz
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)(4)	IDD	—	1.8	2.4	mA	FOSC = 4 MHz, VDD = 5.5V, XT mode
		—	2.6	3.6	mA	FOSC = 10 MHz, VDD = 3.0V, HS mode
		—	4.5	16	mA	FOSC = 20 MHz, VDD = 5.5V, HS mode
		—	14	32	µA	FOSC = 32 kHz, VDD = 3.0V, LP mode, Commercial
		—	17	40	µA	FOSC = 32 kHz, VDD = 3.0V, LP mode, Industrial
Power-down Current(5)	IPD	—	0.25	4.0	µA	VDD = 3.0V, WDT disabled, Commercial
		—	0.25	5.0	µA	VDD = 3.0V, WDT disabled, Industrial
		—	1.8	7.0	µA	VDD = 5.5V, WDT disabled, Commercial
		—	2.0	8.0	µA	VDD = 5.5V, WDT disabled, Industrial
Watchdog Timer Current	ΔIWDT	—	3.75	8.0	µA	VDD = 3.0V, Commercial
		—	3.75	9.0	µA	VDD = 3.0V, Industrial
		—	8	20	µA	VDD = 5.5V*, Commercial
		—	10	22	µA	VDD = 5.5V*, Industrial

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

15.2 DC Characteristics: PIC16C54C/C55A/C56A/C57C/C58B-04E, 20E (Extended) PIC16CR54C/CR56A/CR57C/CR58B-04E, 20E (Extended)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature –40°C ≤ TA ≤ +125°C (extended)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage	VDD					
XT, RC, LP and HS options		3.0	—	5.5	V	HS Option from 0 - 10MHz
HS option		4.5	—	5.5	V	HS Option from 0 - 20MHz
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)	IDD					
XT and RC(4) options		—	1.8	3.3	mA	FOSC = 4.0 MHz, VDD = 5.5V
HS option		—	9.0	20	mA	FOSC = 20 MHz, VDD = 5.5V
Power-down Current(5)	IPD	—	0.3	17	µA	VDD = 3.0V, WDT disabled
		—	10	50	µA	VDD = 4.5V, WDT disabled
		—	12	60	µA	VDD = 5.5V, WDT disabled
Watchdog Timer Current	ΔIWDT	—	4.5	14	µA	VDD = 3.0V
		—	8	18	µA	VDD = 4.5V*
			14	30	µA	VDD = 5.5V*

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

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15.3 DC Characteristics: PIC16LC5X-04, PIC16LCR5X-04 (Commercial) PIC16LC5X-04I, PIC16LCR5X-04I (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Supply Voltage XT and RC options LP options	VDD	 3.0 2.5	 — —	 5.5 5.5	 V V	
RAM Data Retention Voltage(2)	VDR	—	1.5*	—	V	Device in SLEEP mode
VDD start voltage to ensure Power-on Reset	VPOR	—	VSS	—	V	See Section 7.4 for details on Power-on Reset
VDD rise rate to ensure Power-on Reset	SVDD	0.05*	—	—	V/ms	See Section 7.4 for details on Power-on Reset
Supply Current(3)(4)	IDD	— — — —	0.4 0.5 11 14	0.6 2.4 27 35	mA mA µA µA	FOSC = 4.0 MHz, VDD = 2.5V, XT mode FOSC = 4.0 MHz, VDD = 5.5V, XT mode FOSC = 32 kHz, VDD = 2.5V, LP mode, Commercial FOSC = 32 kHz, VDD = 2.5V, LP mode, Industrial
Power-down Current(5)	IPD	— —	0.25 0.25	2 3	µA µA	VDD = 2.5V, WDT disabled, Commercial VDD = 2.5V, WDT disabled, Industrial
Watchdog Timer Current	ΔIWDT	— —	0.8 1	3 5	µA µA	VDD = 2.5V, Commercial VDD = 2.5V, Industrial

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kΩ.

5: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.

15.4 DC Characteristics: PIC16C54B/C54C/C55A/C56A/C57C/C58B-04, 20 (Commercial, Industrial, Extended) PIC16LC54B/LC54C/LC55A/LC56A/LC57C/LC58B-04 (Commercial, Industrial) PIC16CR54C/CR56A/CR57C/CR58B-04, 20 (Commercial, Industrial, Extended) PIC16LCR54B/LCR54C/LCR56A/LCR57C/LCR58B-04 (Commercial, Industrial)

DC Characteristics All Pins Except Power Supply Pins	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.					
Characteristic	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
Input Low Voltage	VIL					
I/O Ports		VSS	—	0.8 V	V	4.5V <VDD ≤ 5.5V
I/O Ports		VSS	—	0.15 VDD	V	Otherwise
$\overline{\text{MCLR}}$ (Schmitt Trigger)		VSS	—	0.15 VDD	V	
T0CKI (Schmitt Trigger)		VSS	—	0.15 VDD	V	
OSC1 (Schmitt Trigger)		VSS	—	0.15 VDD	V	RC option only(4)
OSC1				0.3 VDD	—	XT, HS and LP options
Input High Voltage	VIH					
		2.0	—	VDD	V	4.5V < VDD ≤ 5.5V
I/O ports		0.25 VDD+0.8V	—	VDD	V	Otherwise
$\overline{\text{MCLR}}$ (Schmitt Trigger)		0.85 VDD	—	VDD	V	
T0CKI (Schmitt Trigger)		0.85 VDD	—	VDD	V	
OSC1 (Schmitt Trigger)		0.85 VDD	—	VDD	V	RC option only(4)
OSC1		0.7 VDD	—	VDD	V	XT, HS and LP options
Hysteresis of Schmitt Trigger inputs	VHYS	0.15VDD*	—	—	V	
Input Leakage Current(3)	IIL					**For VDD ≤ 5.5V**
I/O ports		-1.0	0.5	+1.0	µA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
$\overline{\text{MCLR}}$		-5.0	—	+5.0	µA	VPIN = VSS +0.25V(2)
			0.5	+3.0	µA	VPIN = VDD(2)
T0CKI		-3.0	0.5	+3.0	µA	VSS ≤ VPIN ≤ VDD
OSC1		-3.0	0.5	—	µA	VSS ≤ VPIN ≤ VDD, XT, HS and LP options
Output Low Voltage	VOL					
I/O ports		—	—	0.6	V	IOL = 8.7 mA, VDD = 4.5V
OSC2/CLKOUT		—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V, RC option only
Output High Voltage	VOH					
I/O ports(3)		VDD-0.7	—	—	V	IOH = -5.4 mA, VDD = 4.5V
OSC2/CLKOUT		VDD-0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: The leakage current on the $\overline{\text{MCLR}}$/VPP pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.

3: Negative current is defined as coming out of the pin.

4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C5X be driven with external clock in RC mode.

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15.5 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

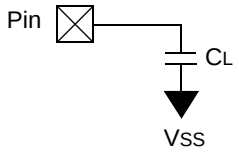
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 15-3: LOAD CONDITIONS - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B, PIC16CR5X



CL = 50 pF for all pins except OSC2
15 pF for OSC2 in XT, HS or LP options when external clock is used to drive OSC1

15.6 Timing Diagrams and Specifications

FIGURE 15-4: EXTERNAL CLOCK TIMING - PIC16C5X, PIC16CR5X

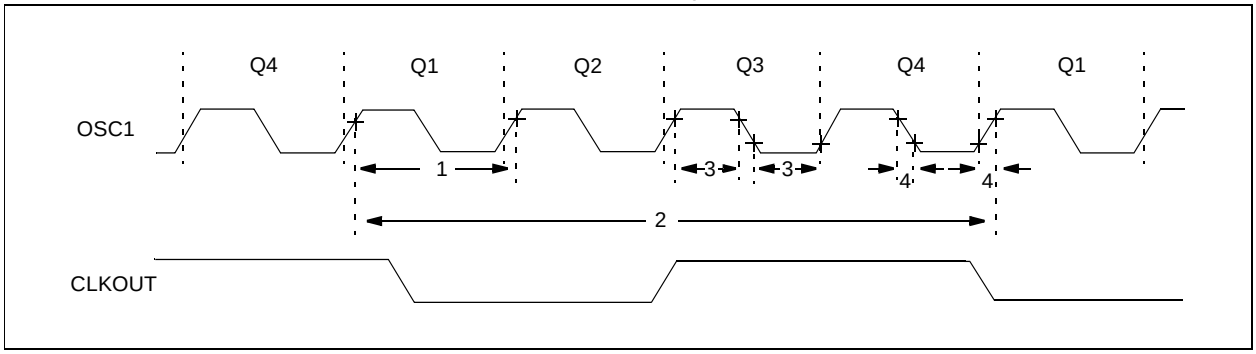


TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
	FOSC	External CLKIN Frequency(2)	DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency(2)	DC	—	4.0	MHz	RC osc mode
			DC	—	4.0	MHz	XT osc mode
			DC	—	4.0	MHz	HS osc mode (04)
			DC	—	20	MHz	HS osc mode (20)
			DC	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT osc mode
			250	—	—	ns	HS osc mode (04)
			50	—	—	ns	HS osc mode (20)
			5.0	—	—	µs	LP osc mode
		Oscillator Period(2)	250	—	—	ns	RC osc mode
			250	—	2,200	ns	XT osc mode
			250	—	250	ns	HS osc mode (04)
			50	—	250	ns	HS osc mode (20)
			5.0	—	200	µs	LP osc mode

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

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TABLE 15-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X (CON'T)

AC Characteristics	Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.

Parameter No.	Sym	Characteristic	Min	Typ(1)	Max	Units	Conditions
2	TCY	Instruction Cycle Time(3)	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			20*	—	—	ns	HS oscillator
			2.0*	—	—	µs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	25*	ns	HS oscillator
			—	—	50*	ns	LP oscillator

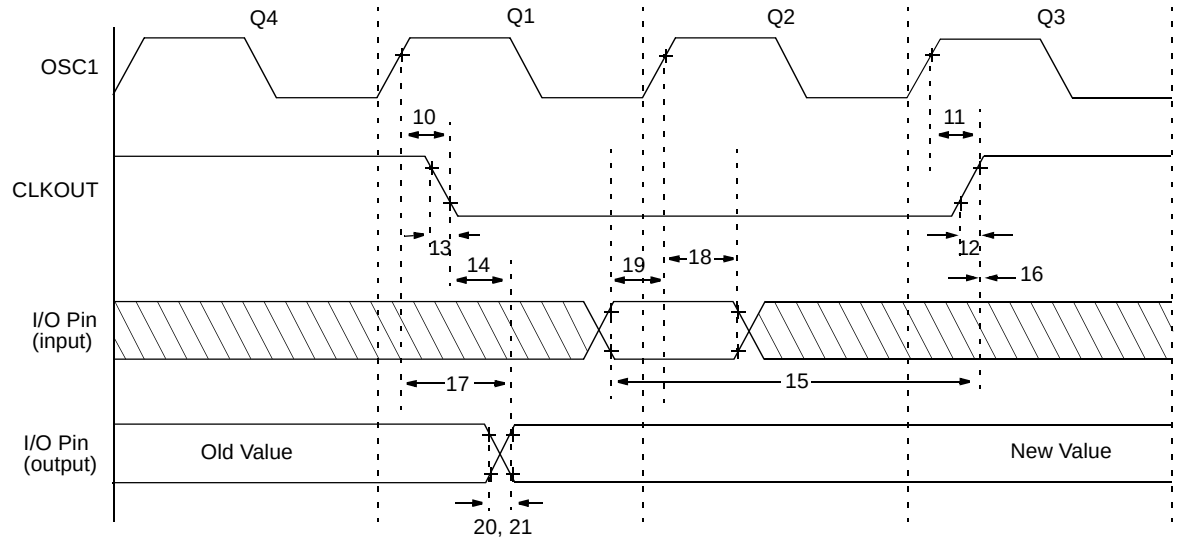
* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.
When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

FIGURE 15-5: CLKOUT AND I/O TIMING - PIC16C5X, PIC16CR5X



Note: Refer to Figure 19-1 for load conditions.

TABLE 15-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.					
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**
10	TosH2ckL	OSC1↑ to CLKOUT↓(2)	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑(2)	—	15	30**	ns
12	TckR	CLKOUT rise time(2)	—	5.0	15**	ns
13	TckF	CLKOUT fall time(2)	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid(2)	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑(2)	0.25 TCY+30*	—	—	ns
16	TckH2ioI	Port in hold after CLKOUT↑(2)	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid(3)	—	—	100*	ns
18	TosH2ioI	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time(3)	—	10	25**	ns
21	TioF	Port output fall time(3)	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 15-3 for loading conditions.

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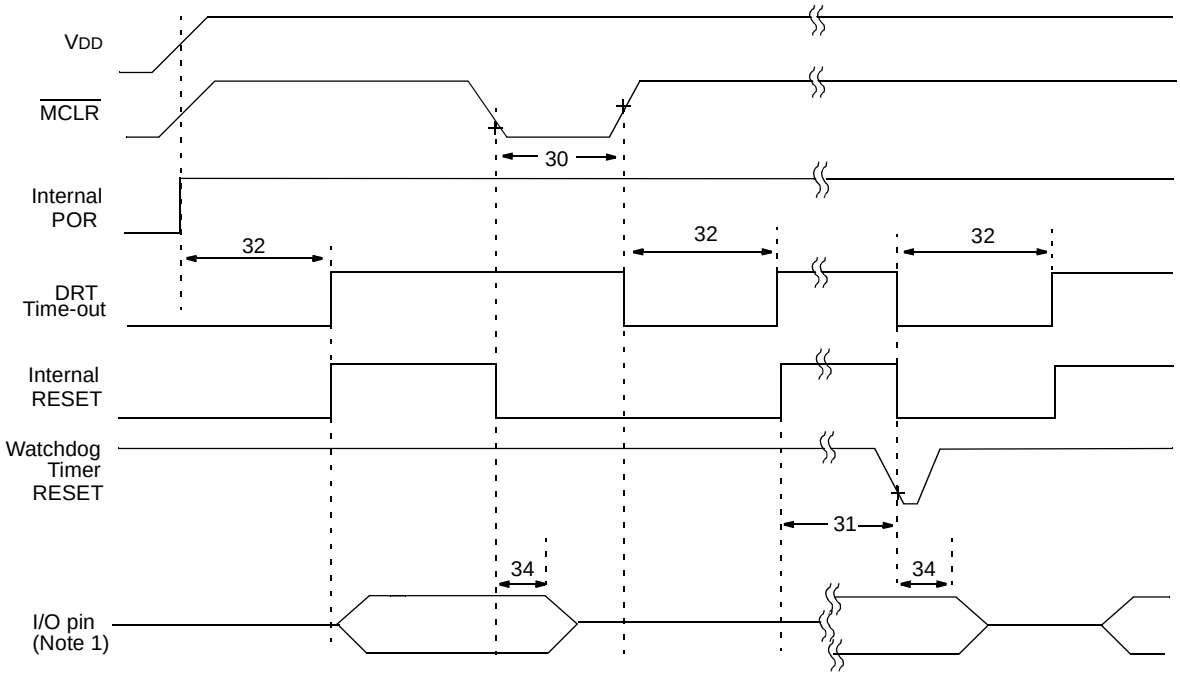
FIGURE 15-6: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16C5X, PIC16CR5X



Note 1: I/O pins must be taken out of hi-impedance mode by enabling the output drivers in software.

TABLE 15-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16C5X, PIC16CR5X

AC Characteristics	**Standard Operating Conditions (unless otherwise specified)** Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.						
Parameter No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
30	TmcL	$\overline{\text{MCLR}}$ Pulse Width (low)	1000*	—	—	ns	VDD = 5.0V
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	VDD = 5.0V (Commercial)
34	Tioz	I/O Hi-impedance from $\overline{\text{MCLR}}$ Low	100*	300*	1000*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 15-7: TIMER0 CLOCK TIMINGS - PIC16C5X, PIC16CR5X

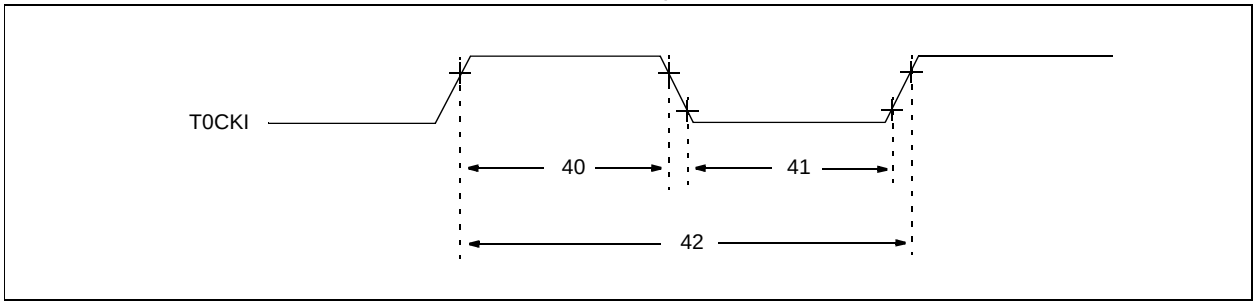


TABLE 15-4: TIMER0 CLOCK REQUIREMENTS - PIC16C5X, PIC16CR5X

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended) Operating Voltage VDD range is described in Section 15.1, Section 15.2 and Section 15.3.				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
40	Tt0H	T0CKI High Pulse Width- No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	0.5 TCY + 20*	—	—	ns	
		- With Prescaler	10*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40}{N}$*	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4,..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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16.0 DC AND AC CHARACTERISTICS - PIC16C54C/CR54C/C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B

The graphs and tables provided in this section are for design guidance and are not tested. In some graphs or tables, the data presented is outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. “Typical” represents the mean of the distribution, while “max” or “min” represents (mean + 3σ) and (mean – 3σ) respectively, where σ is standard deviation.

FIGURE 16-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

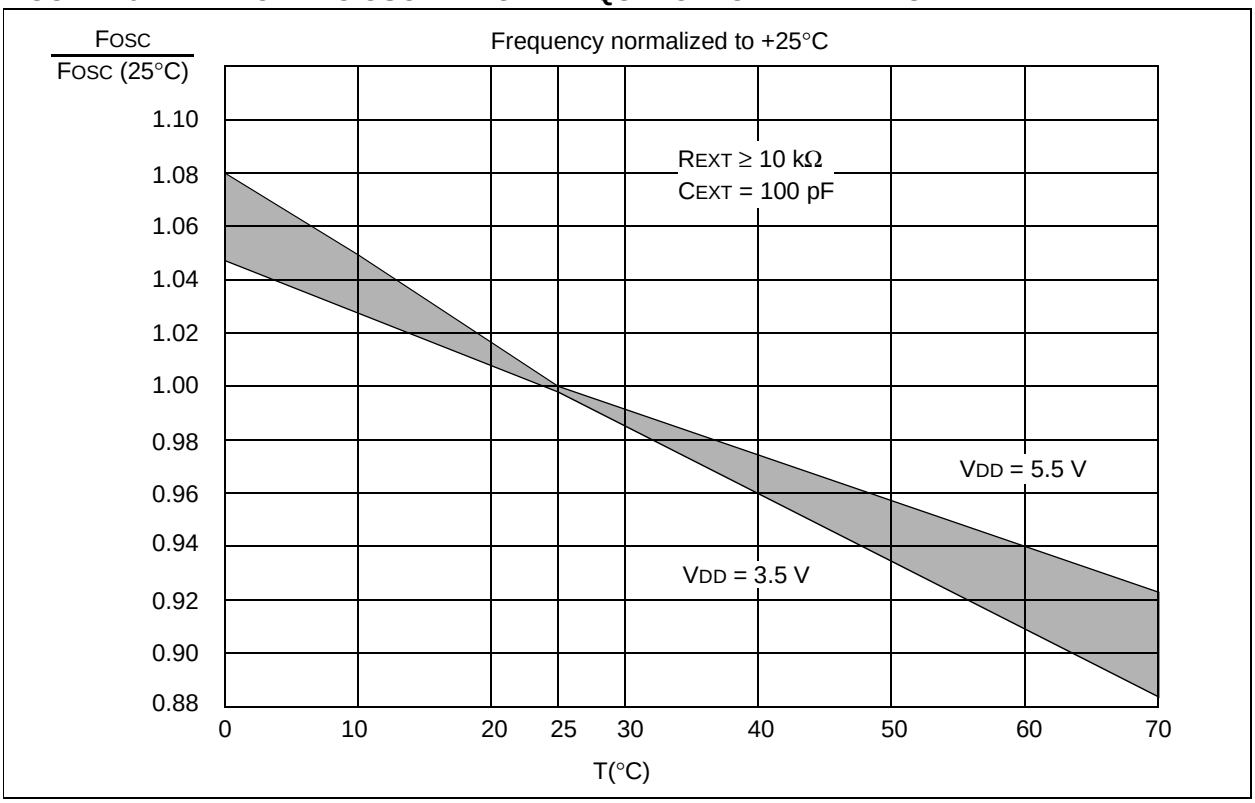

TABLE 16-1: RC OSCILLATOR FREQUENCIES

CEXT	REXT	Average Fosc @ 5 V, 25°C	
20 pF	3.3 k	4.973 MHz	± 27%
	5 k	3.82 MHz	± 21%
	10 k	2.22 MHz	± 21%
	100 k	262.15 kHz	± 31%
100 pF	3.3 k	1.63 MHz	± 13%
	5 k	1.19 MHz	± 13%
	10 k	684.64 kHz	± 18%
	100 k	71.56 kHz	± 25%
300 pF	3.3 k	660 kHz	± 10%
	5.0 k	484.1 kHz	± 14%
	10 k	267.63 kHz	± 15%
	160 k	29.44 kHz	± 19%

The frequencies are measured on DIP packages.

The percentage variation indicated here is part-to-part variation due to normal process distribution. The variation indicated is ±3 standard deviation from average value for VDD = 5 V.

FIGURE 16-2: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 20 pF

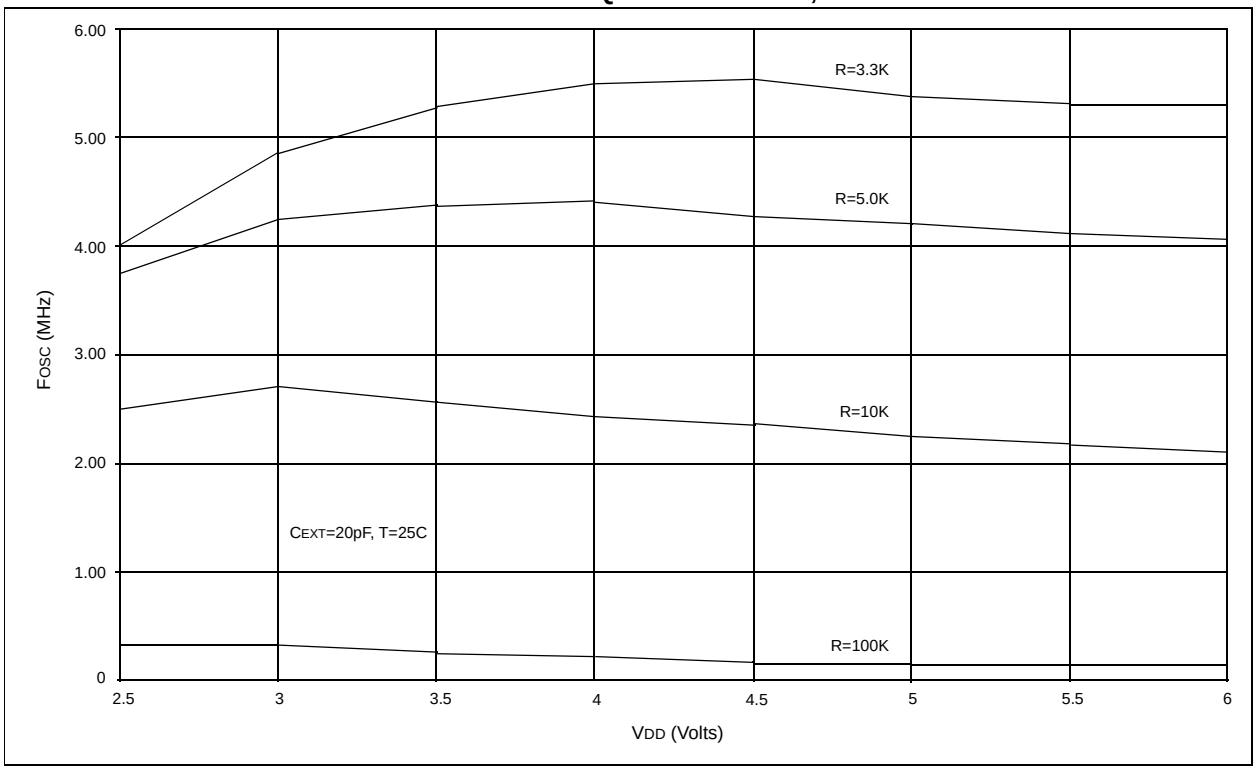

FIGURE 16-3: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 100 pF

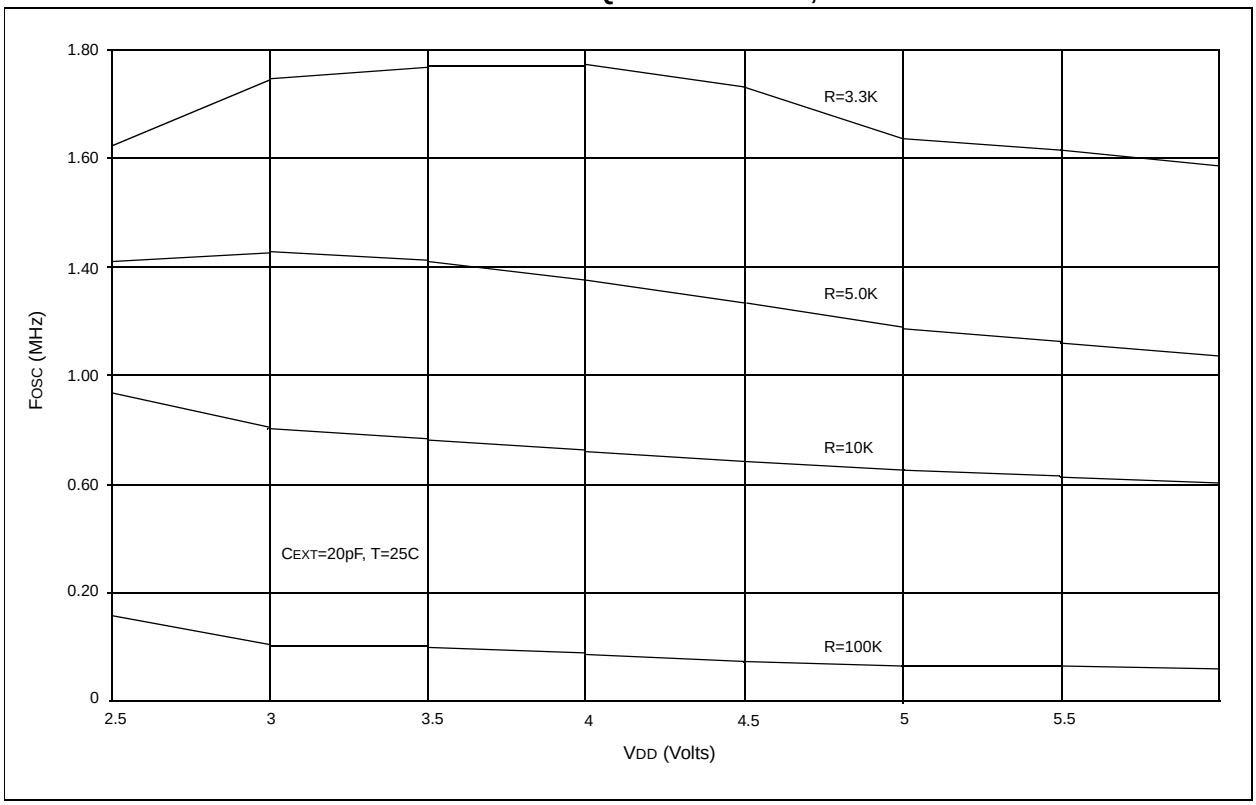

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FIGURE 16-4: TYPICAL RC OSCILLATOR FREQUENCY vs. VDD, CEXT = 300 pF

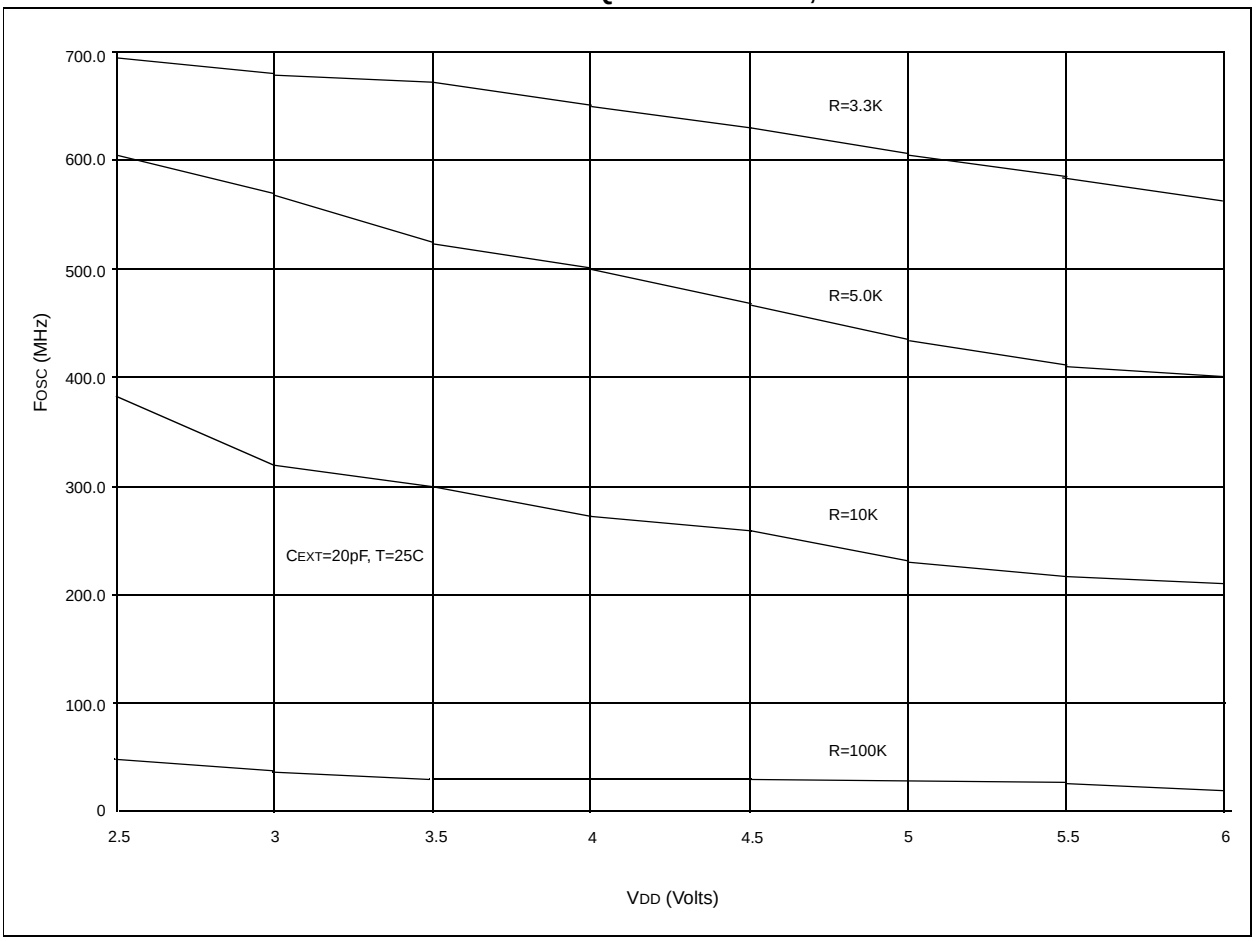

FIGURE 16-5: TYPICAL IPD vs. VDD, WATCHDOG DISABLED (25°C)

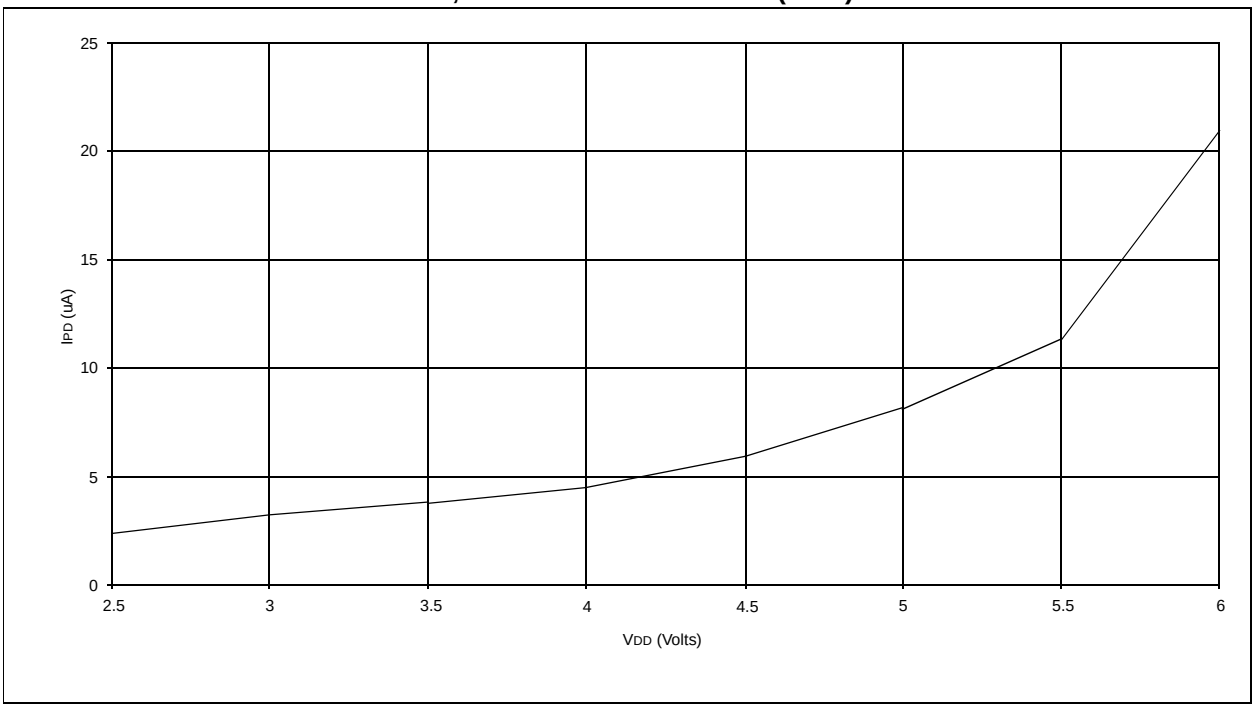

FIGURE 16-6: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (25°C)

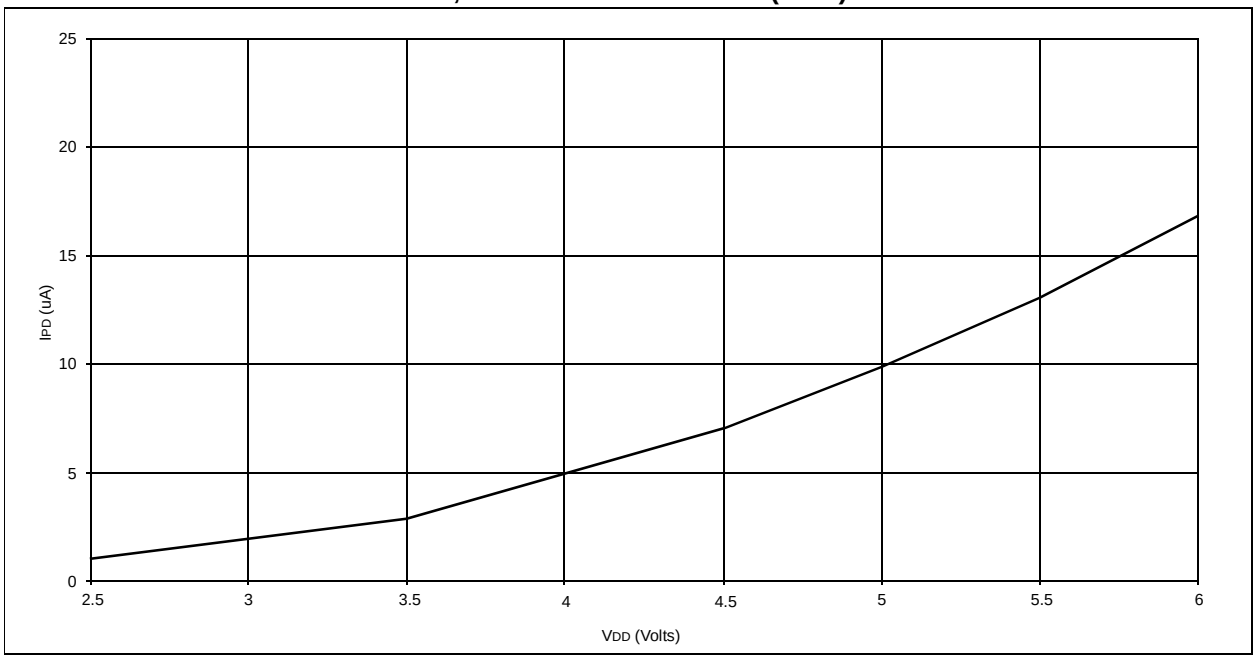

FIGURE 16-7: TYPICAL IPD vs. VDD, WATCHDOG ENABLED (–40°C, 85°C)

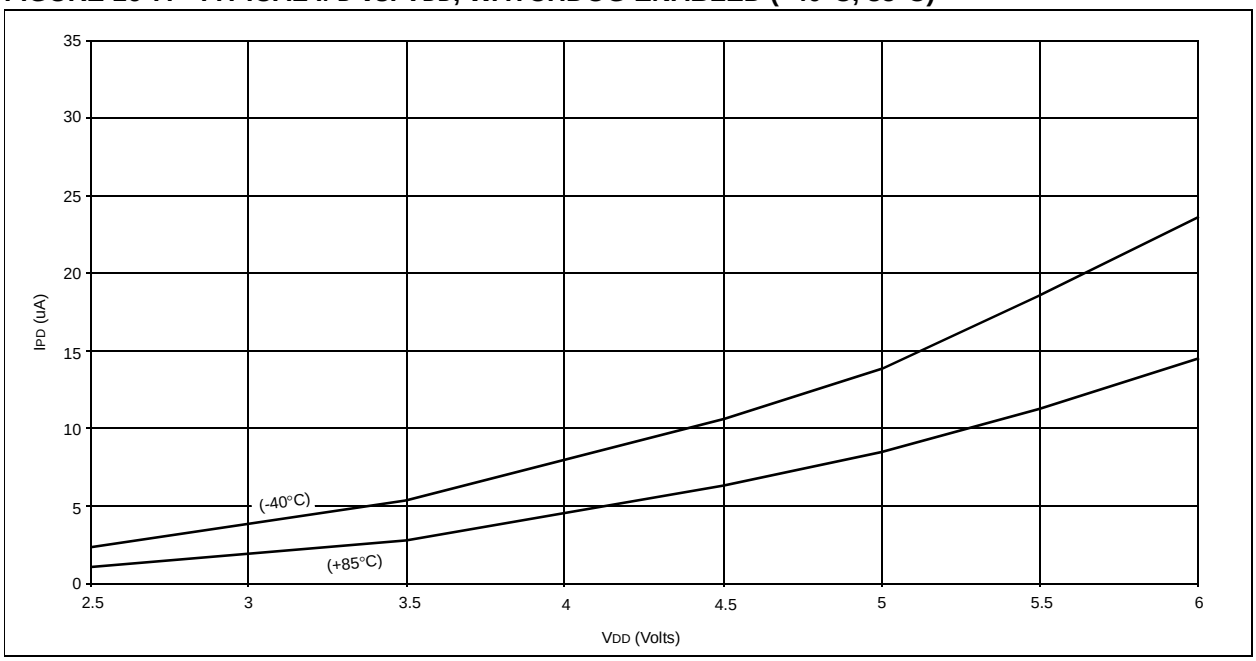

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FIGURE 16-8: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF I/O PINS vs. VDD

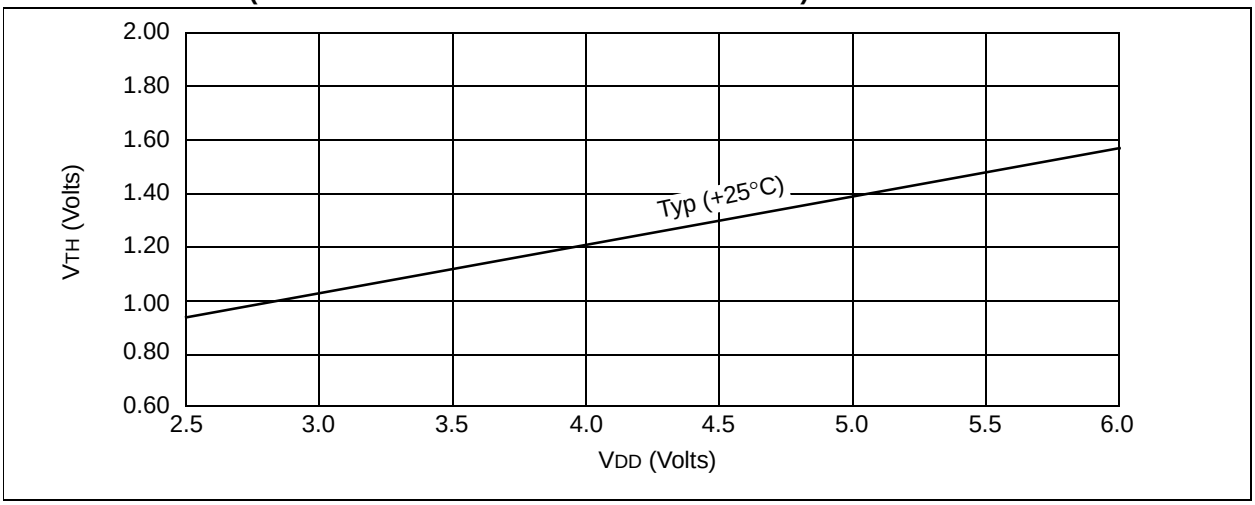
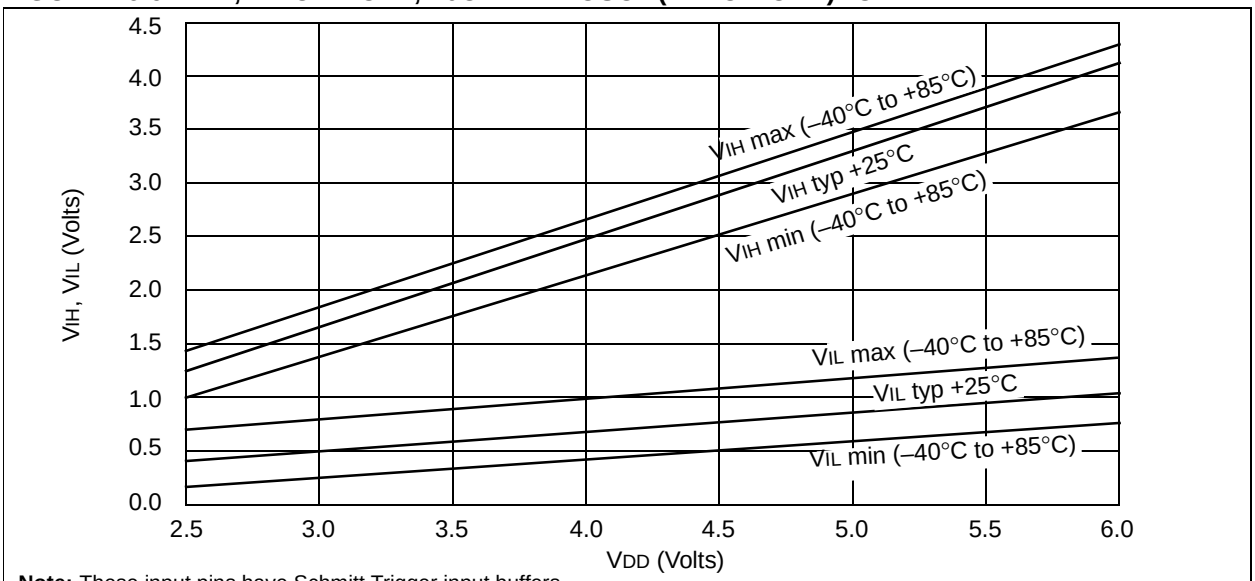


FIGURE 16-9: VIH, VIL OF $\overline{\text{MCLR}}$, T0CKI AND OSC1 (IN RC MODE) vs. VDD



Note: These input pins have Schmitt Trigger input buffers.

FIGURE 16-10: VTH (INPUT THRESHOLD TRIP POINT VOLTAGE) OF OSC1 INPUT (IN XT, HS AND LP MODES) vs. VDD

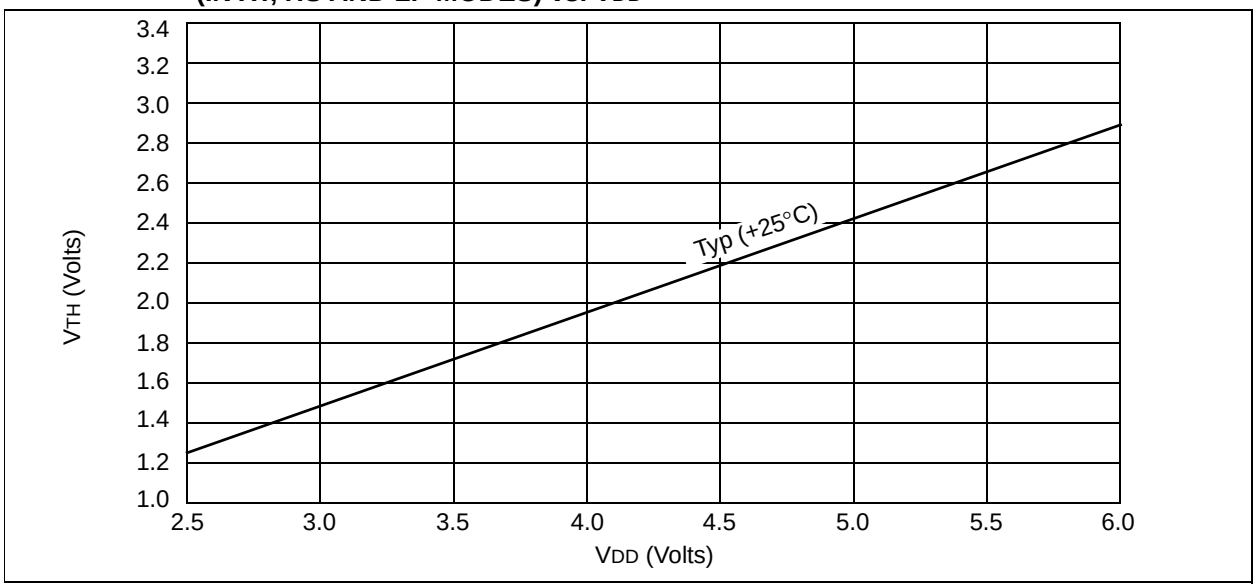


FIGURE 16-11: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 20 pF, 25°C)

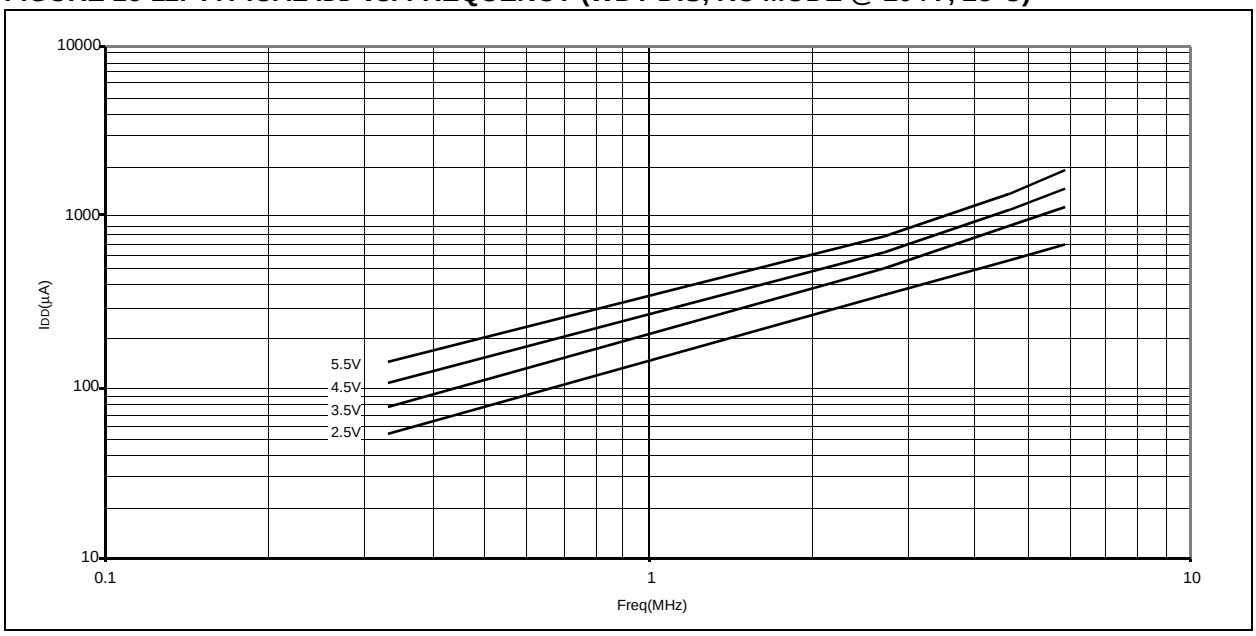


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FIGURE 16-12: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 100 pF, 25°C)

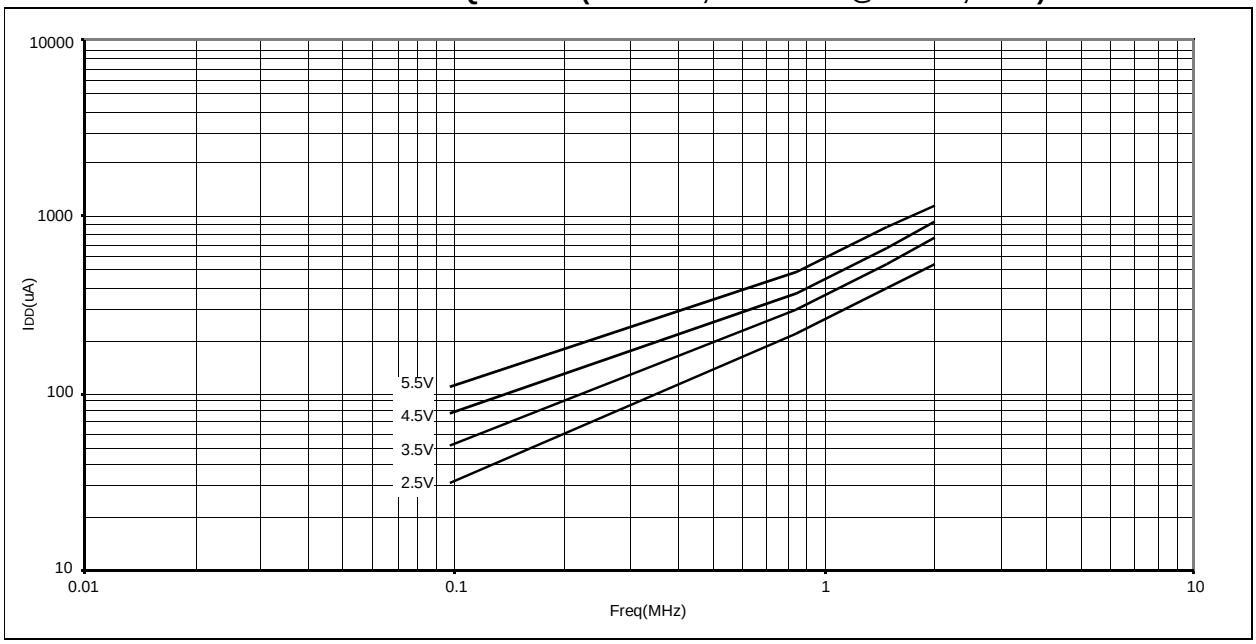

FIGURE 16-13: TYPICAL IDD vs. FREQUENCY (WDT DIS, RC MODE @ 300 pF, 25°C)

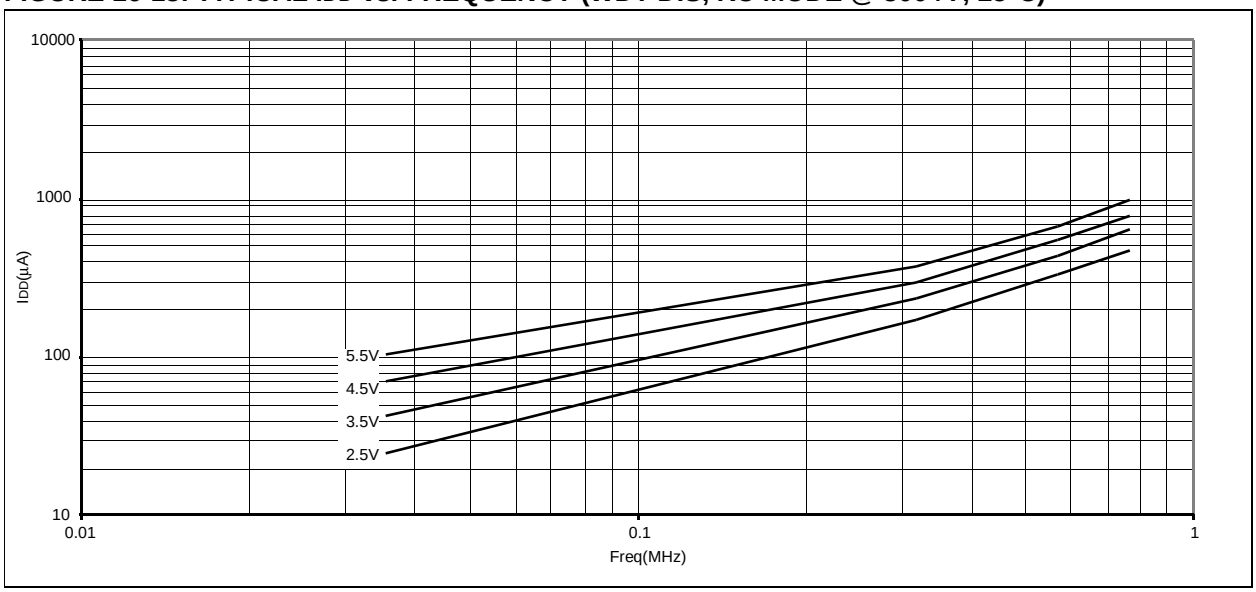

FIGURE 16-14: WDT TIMER TIME-OUT PERIOD vs. VDD

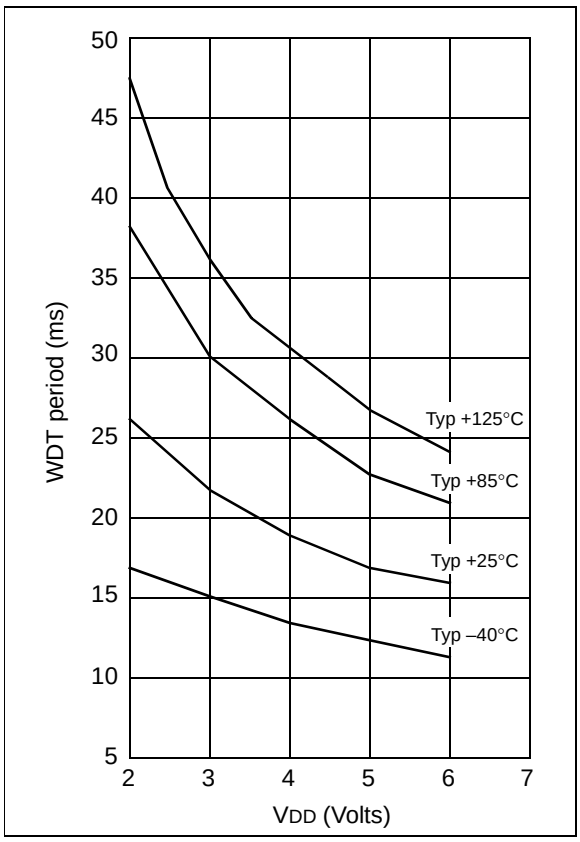

TABLE 16-2: INPUT CAPACITANCE

Pin	Typical Capacitance (pF)	
	18L PDIP	18L SOIC
RA port	5.0	4.3
RB port	5.0	4.3
$\overline{MCLR}$	17.0	17.0
OSC1	4.0	3.5
OSC2/CLKOUT	4.3	3.5
T0CKI	3.2	2.8

All capacitance values are typical at 25°C. A part-to-part variation of ±25% (three standard deviations) should be taken into account.

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FIGURE 16-15: I_{OH} vs. V_{OH}, V_{DD} = 3 V

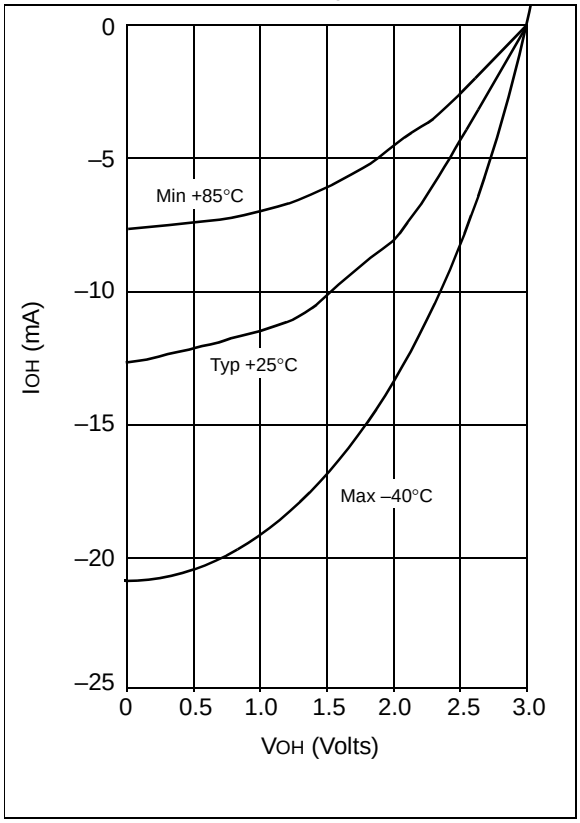


FIGURE 16-16: I_{OH} vs. V_{OH}, V_{DD} = 5 V

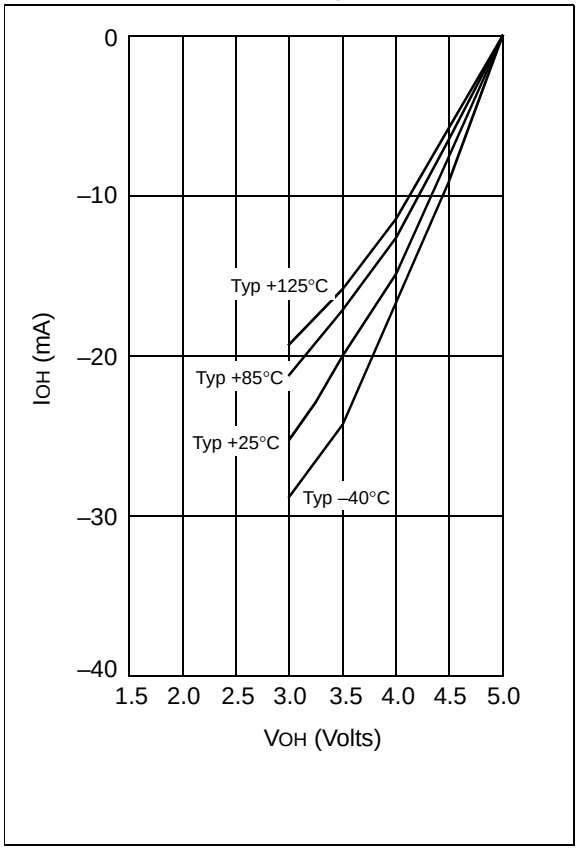


FIGURE 16-17: I_{OL} vs. V_{OL}, V_{DD} = 3 V

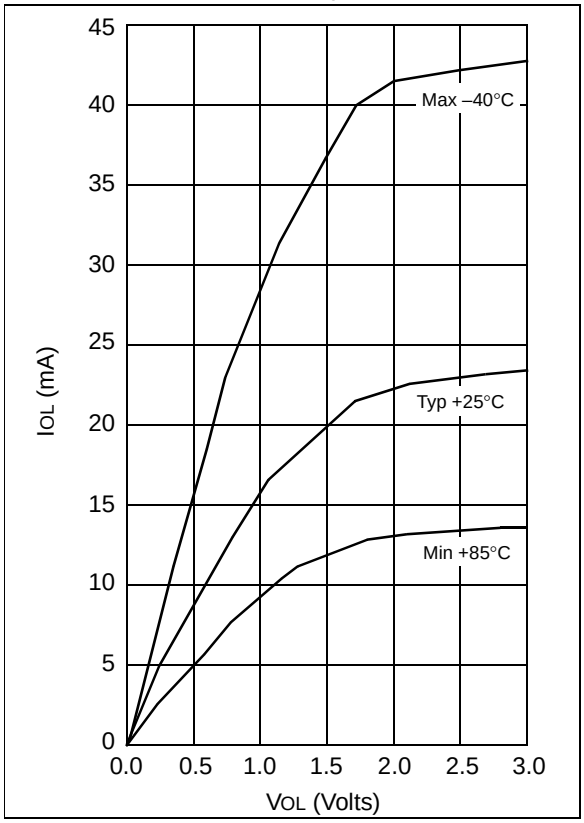
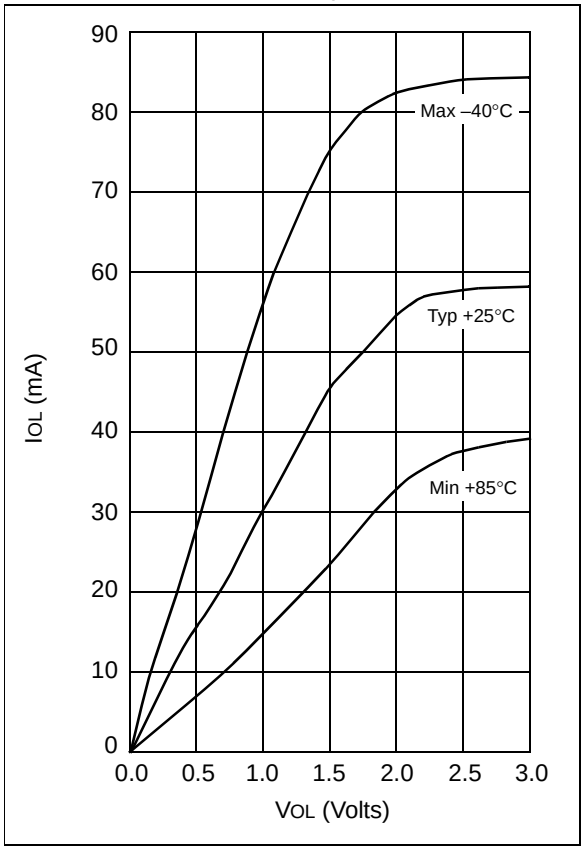


FIGURE 16-18: I_{OL} vs. V_{OL}, V_{DD} = 5 V



NOTES:

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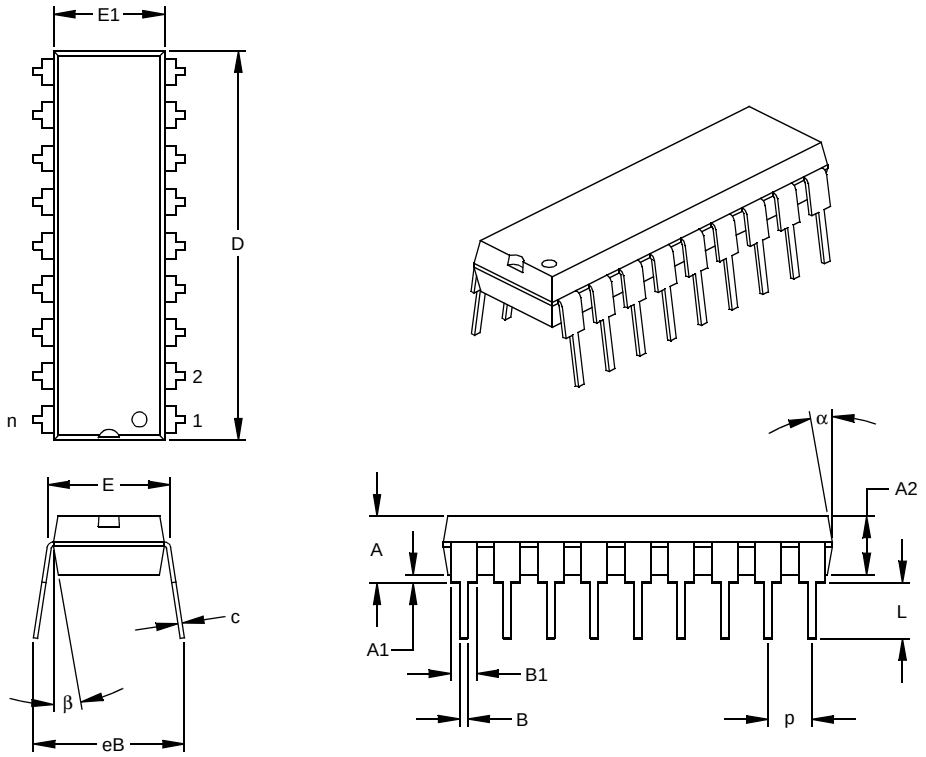
17.0 PACKAGING INFORMATION

18-Lead Plastic Dual In-line (P) – 300 mil (PDIP)

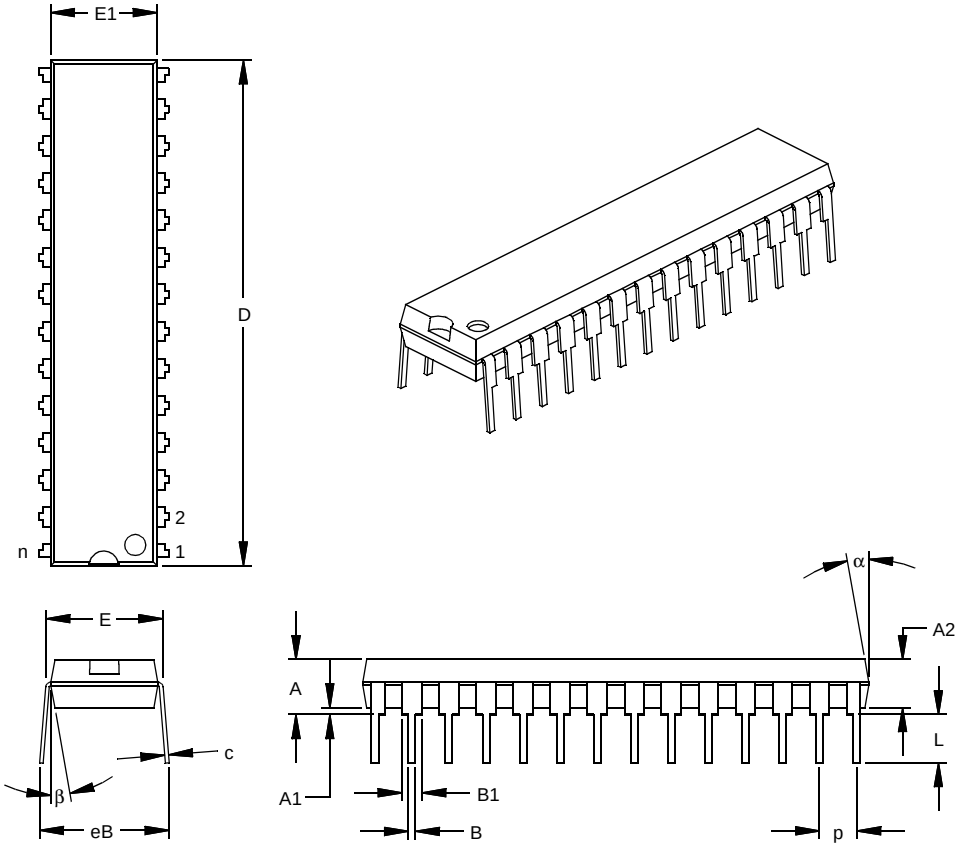


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.890	.898	.905	22.61	22.80	22.99
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-007

28-Lead Skinny Plastic Dual In-line (SP) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.140	.150	.160	3.56	3.81	4.06
Molded Package Thickness	A2	.125	.130	.135	3.18	3.30	3.43
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.310	.325	7.62	7.87	8.26
Molded Package Width	E1	.275	.285	.295	6.99	7.24	7.49
Overall Length	D	1.345	1.365	1.385	34.16	34.67	35.18
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.040	.053	.065	1.02	1.33	1.65
Lower Lead Width	B	.016	.019	.022	0.41	0.48	0.56
Overall Row Spacing §	eB	.320	.350	.430	8.13	8.89	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimension D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-095
Drawing No. C04-070

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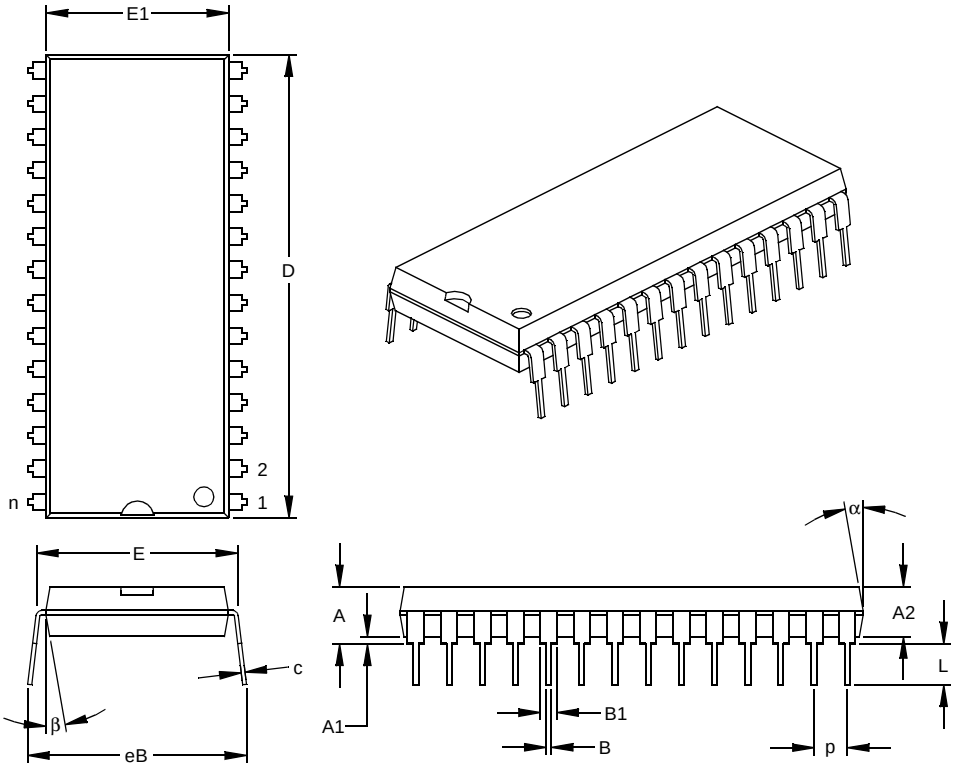
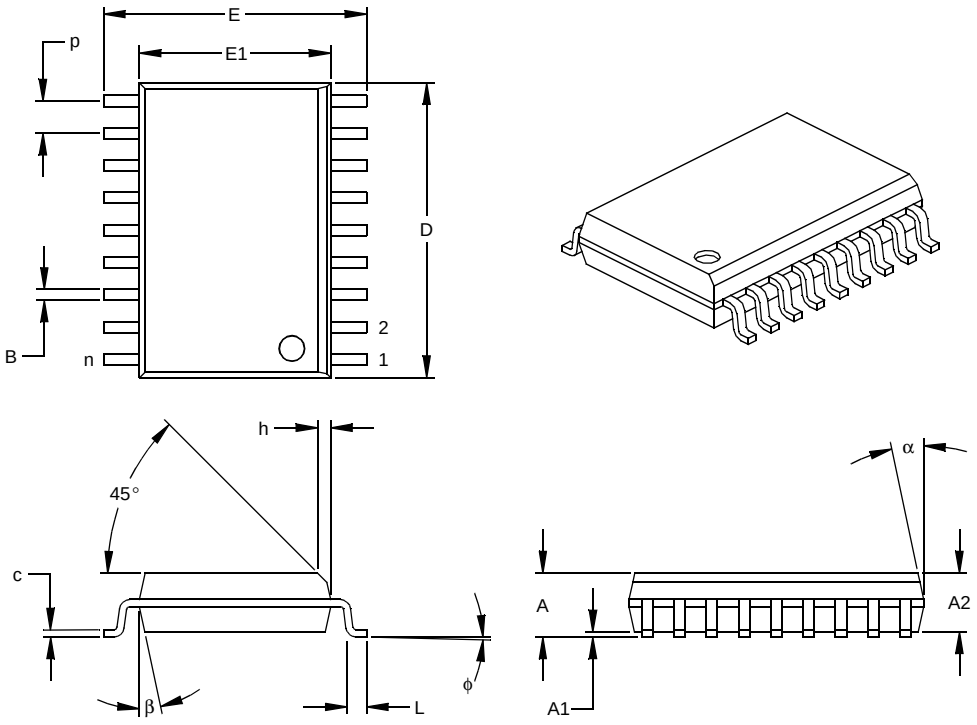
28-Lead Plastic Dual In-line (P) – 600 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.175	.190	4.06	4.45	4.83
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.505	.545	.560	12.83	13.84	14.22
Overall Length	D	1.395	1.430	1.465	35.43	36.32	37.21
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-011
Drawing No. C04-079

18-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.291	.295	.299	7.39	7.49	7.59
Overall Length	D	.446	.454	.462	11.33	11.53	11.73
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.012	0.23	0.27	0.30
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-051

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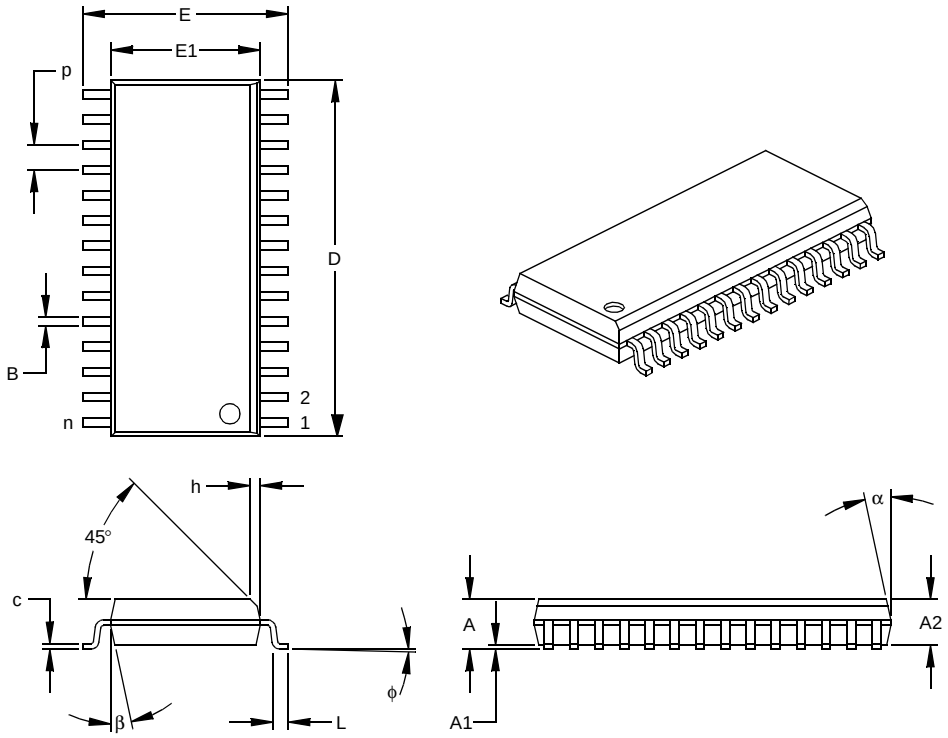
28-Lead Plastic Small Outline (SO) – Wide, 300 mil (SOIC)

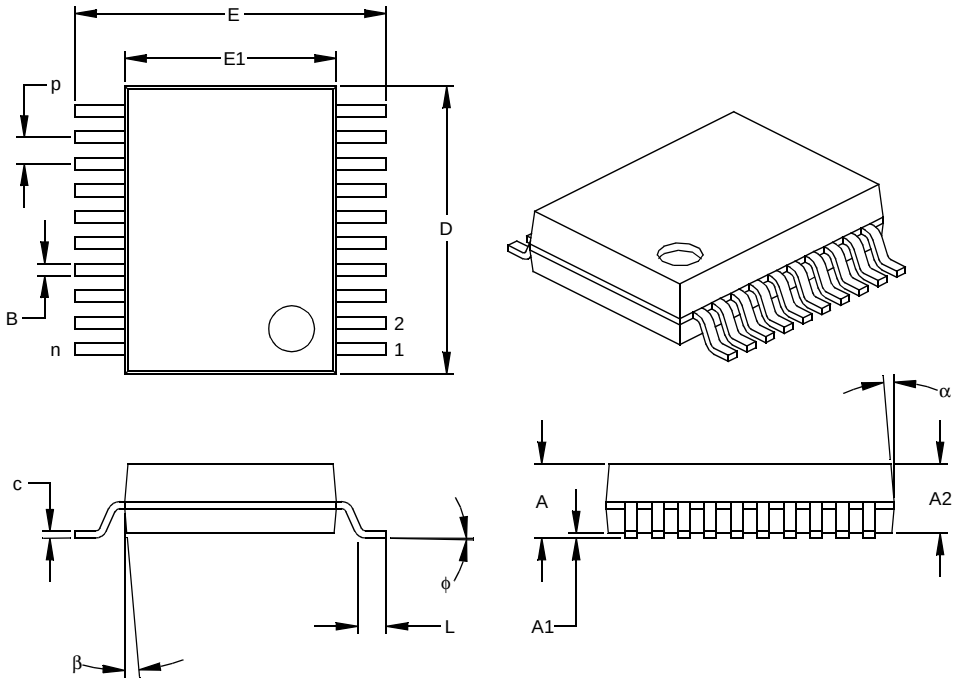


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.050			1.27	
Overall Height	A	.093	.099	.104	2.36	2.50	2.64
Molded Package Thickness	A2	.088	.091	.094	2.24	2.31	2.39
Standoff §	A1	.004	.008	.012	0.10	0.20	0.30
Overall Width	E	.394	.407	.420	10.01	10.34	10.67
Molded Package Width	E1	.288	.295	.299	7.32	7.49	7.59
Overall Length	D	.695	.704	.712	17.65	17.87	18.08
Chamfer Distance	h	.010	.020	.029	0.25	0.50	0.74
Foot Length	L	.016	.033	.050	0.41	0.84	1.27
Foot Angle Top	ϕ	0	4	8	0	4	8
Lead Thickness	c	.009	.011	.013	0.23	0.28	0.33
Lead Width	B	.014	.017	.020	0.36	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-013
Drawing No. C04-052

20-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.322	7.59	7.85	8.18
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.278	.284	.289	7.06	7.20	7.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	c	.004	.007	.010	0.10	0.18	0.25
Foot Angle	φ	0	4	8	0.00	101.60	203.20
Lead Width	B	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-150
Drawing No. C04-072

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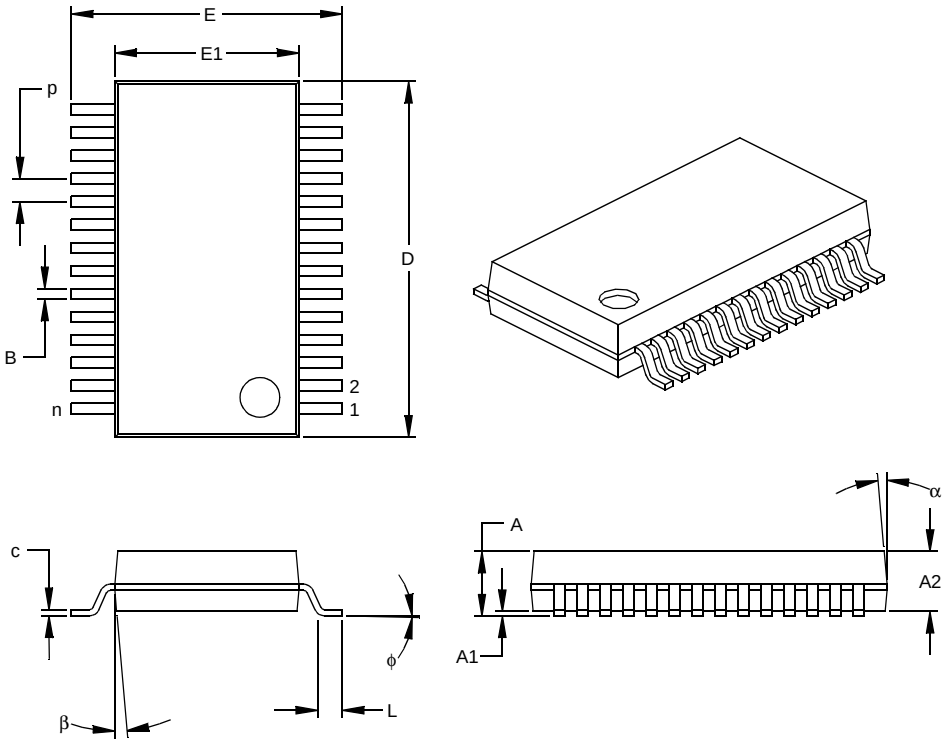
28-Lead Plastic Shrink Small Outline (SS) – 209 mil, 5.30 mm (SSOP)

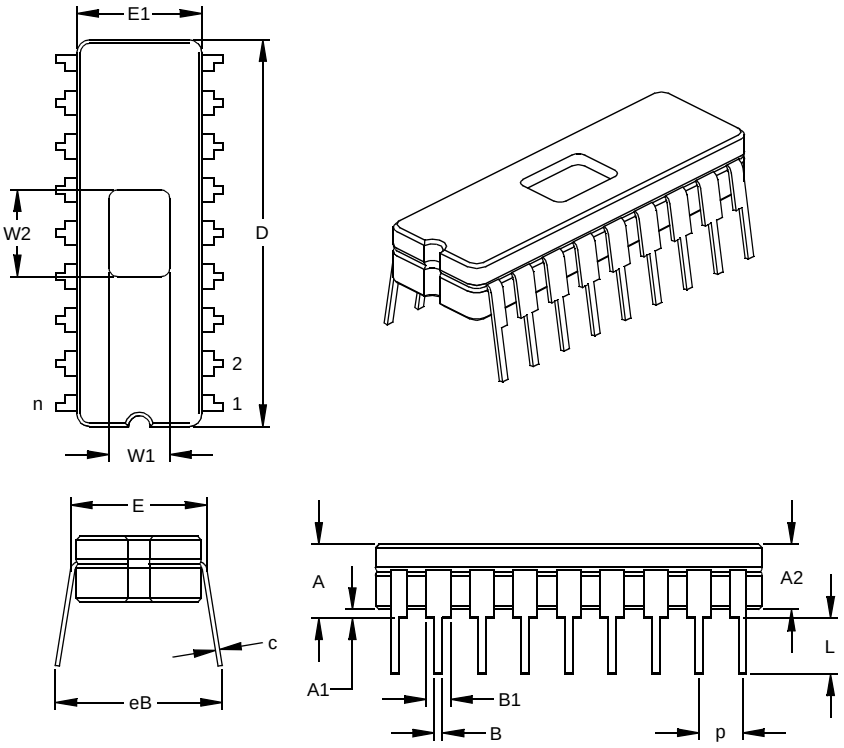


Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.026			0.65	
Overall Height	A	.068	.073	.078	1.73	1.85	1.98
Molded Package Thickness	A2	.064	.068	.072	1.63	1.73	1.83
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Overall Width	E	.299	.309	.319	7.59	7.85	8.10
Molded Package Width	E1	.201	.207	.212	5.11	5.25	5.38
Overall Length	D	.396	.402	.407	10.06	10.20	10.34
Foot Length	L	.022	.030	.037	0.56	0.75	0.94
Lead Thickness	c	.004	.007	.010	0.10	0.18	0.25
Foot Angle	φ	0	4	8	0.00	101.60	203.20
Lead Width	B	.010	.013	.015	0.25	0.32	0.38
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-150
Drawing No. C04-073

18-Lead Ceramic Dual In-line with Window (JW) – 300 mil (CERDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		18			18	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.170	.183	.195	4.32	4.64	4.95
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.023	.030	0.38	0.57	0.76
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Ceramic Pkg. Width	E1	.285	.290	.295	7.24	7.37	7.49
Overall Length	D	.880	.900	.920	22.35	22.86	23.37
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	c	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.055	.060	1.27	1.40	1.52
Lower Lead Width	B	.016	.019	.021	0.41	0.47	0.53
Overall Row Spacing §	eB	.345	.385	.425	8.76	9.78	10.80
Window Width	W1	.130	.140	.150	3.30	3.56	3.81
Window Length	W2	.190	.200	.210	4.83	5.08	5.33

* Controlling Parameter
§ Significant Characteristic
JEDEC Equivalent: MO-036
Drawing No. C04-010

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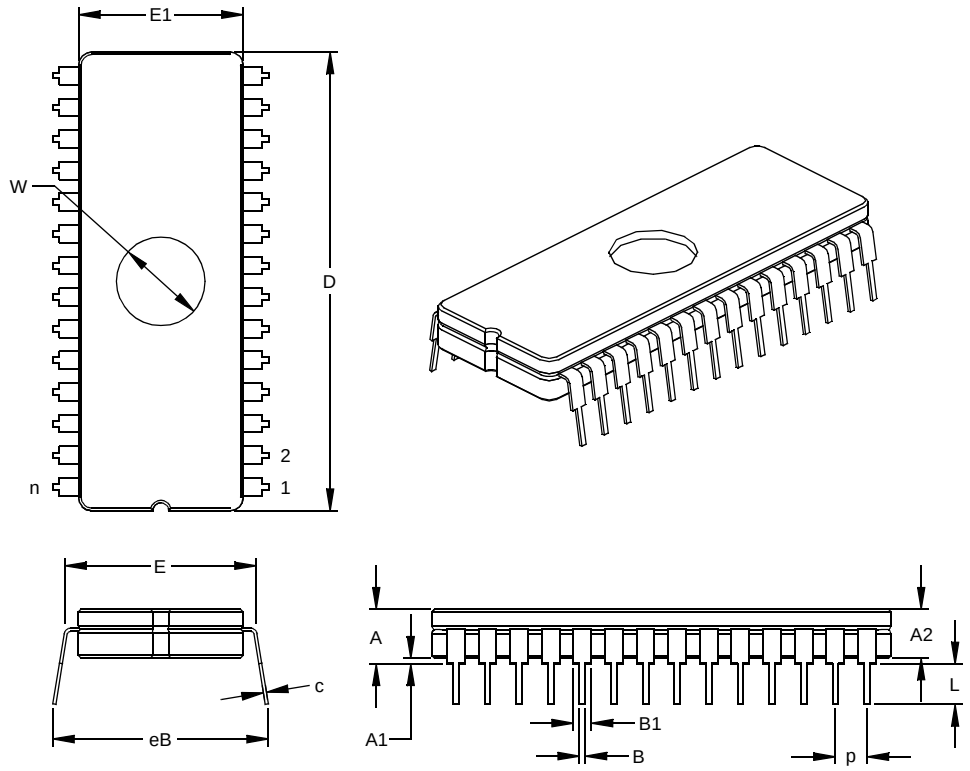
28-Lead Ceramic Dual In-line with Window (JW) – 600 mil (CERDIP)

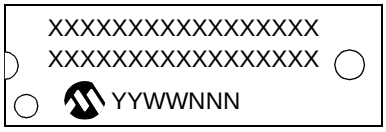


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		28			28	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.170	.185	.200	4.32	4.70	5.08
Ceramic Package Height	A2	.155	.160	.165	3.94	4.06	4.19
Standoff	A1	.015	.038	.060	0.38	0.95	1.52
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Ceramic Pkg. Width	E1	.514	.520	.526	13.06	13.21	13.36
Overall Length	D	1.430	1.460	1.490	36.32	37.08	37.85
Tip to Seating Plane	L	.125	.138	.150	3.18	3.49	3.81
Lead Thickness	c	.008	.010	.012	0.20	0.25	0.30
Upper Lead Width	B1	.050	.058	.065	1.27	1.46	1.65
Lower Lead Width	B	.016	.020	.023	0.41	0.51	0.58
Overall Row Spacing §	eB	.610	.660	.710	15.49	16.76	18.03
Window Diameter	W	.270	.280	.290	6.86	7.11	7.37

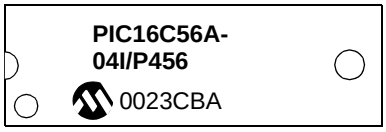
* Controlling Parameter
§ Significant Characteristic
JEDEC Equivalent: MO-103
Drawing No. C04-013

17.1 Package Marking Information

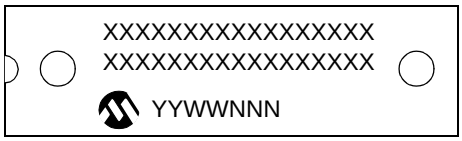
18-Lead PDIP



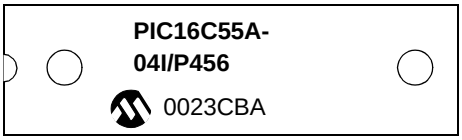
Example



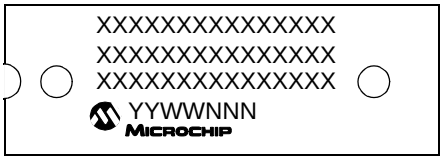
28-Lead Skinny PDIP (.300")



Example



28-Lead PDIP (.600")

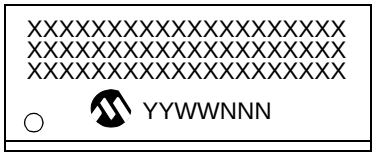


Example

18-Lead SOIC

Example

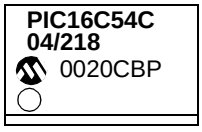
28-Lead SOIC



Example

20-Lead SSOP

Example



28-Lead SSOP

Example

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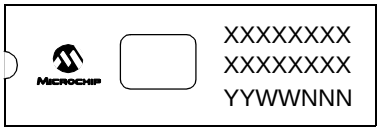
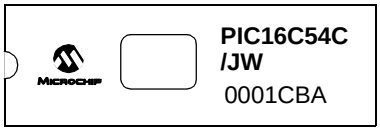
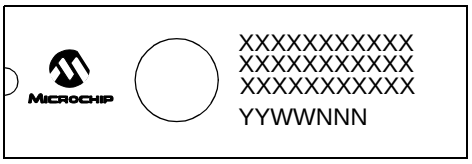
18-Lead CERDIP Windowed



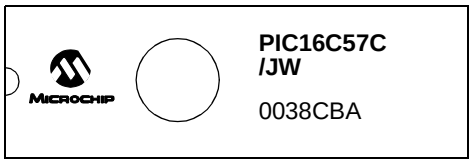
Example



28-Lead CERDIP Windowed



Example



Legend:	XX...X	Customer specific information*
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

***** Standard OTP marking consists of Microchip part number, year code, week code, facility code, mask rev#, and assembly code. For OTP marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

NOTES:

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APPENDIX A: COMPATIBILITY

To convert code written for PIC16CXX to PIC16C5X, the user should take the following steps:

1. Check any `CALL`, `GOTO` or instructions that modify the PC to determine if any program memory page select operations (PA2, PA1, PA0 bits) need to be made.
2. Revisit any computed jump operations (write to PC or add to PC, etc.) to make sure page bits are set properly under the new scheme.
3. Eliminate any special function register page switching. Redefine data variables to reallocate them.
4. Verify all writes to STATUS, OPTION, and FSR registers since these have changed.
5. Change Reset vector to proper value for processor used.
6. Remove any use of the `ADDLW` and `SUBLW` instructions.
7. Rewrite any code segments that use interrupts.

NOTES:

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INDEX

A

Absolute Maximum Ratings 61, 81, 93, 115
ALU 9
Applications 5
Architectural Overview 9
Assembler
    MPASM Assembler 55

B

Block Diagram
    On-Chip Reset Circuit 36
    PIC16C5X Series 10
    Timer0 27
    TMR0/WDT Prescaler 30
    Watchdog Timer 40
Brown-out Protection Circuit 41

C

Carry bit 9
Clocking Scheme 13
CMOS Technology 1
Code Protection 31, 42
Configuration Bits 31
Configuration Word 31
    PIC16C54/C54A/C55/C56/C57 32
    PIC16CR54A/C54C/CR54C/C55A/C56A/
    CR56A/C57C/CR57C/C58B/CR58B 31

D

DC and AC Characteristics - PIC16C54/55/56/57 73
DC and AC Characteristics - PIC16C54A 105
DC and AC Characteristics - PIC16C54C/CR54C/
C55A/C56A/CR56A/C57C/CR57C/C58B/CR58B 127
DC Characteristics 82, 94, 117
    PIC16C54/55/56/57 ..... 62, 63, 64, 65, 66
    PIC16C54A 94
    PIC16CR54A 82
Development Support 55
Device Varieties 7
Digit Carry bit 9

E

Electrical Characteristics
    PIC16C54/55/56/57 61
    PIC16C54A 93
    PIC16C54C/CR54C/C55A/C56A/CR56A/
    C57C/CR57C/C58B/CR58B 115
    PIC16CR54A 81
Errata 4
External Power-on Reset Circuit 37

F

Family of Devices
    PIC16C5X 6
FSR 36
FSR Register 22

H

High-Performance RISC CPU 1

I

I/O Interfacing 25
I/O Ports 25
I/O Programming Considerations 26
ID Locations 31, 42
INDF 36
INDF Register 22
Indirect Data Addressing 22
Instruction Cycle 13
Instruction Flow/Pipelining 13
Instruction Set Summary 43

K

KeeLoq® Evaluation and Programming Tools 58

L

Loading of PC 21, 22

M

$\overline{\text{MCLR}}$ 36
Memory Map 15
    PIC16C54/CR54/C55 15
    PIC16C56/CR56 15
    PIC16C57/CR57/C58/CR58 15
Memory Organization 15
    Data Memory 16
    Program Memory 15
MPLAB Integrated Development Environment Software ... 55

O

One-Time-Programmable (OTP) Devices 7
OPTION 36
OPTION Register 20
OSC selection 31
Oscillator Configurations 33
Oscillator Types
    HS 33
    LP 33
    RC 33
    XT 33

P

Package Marking Information 146
Packaging Information 137
PC 21
PCL 36
Peripheral Features 1
PIC16C54/55/56/57 Product Identification System 156
PIC16C5X Product Identification System 155
PICDEM-1 Low-Cost PICmicro Demo Board 57
PICDEM-2 Low-Cost PIC16CXX Demo Board 57
PICDEM-3 Low-Cost PIC16CXXX Demo Board 57
PICSTART® Plus Entry Level Development System 57
Pin Configurations 2
Pinout Description - PIC16C54s, PIC16CR54, PIC16C56, PIC16CR56, PIC16C58, PIC16CR58 11
Pinout Description - PIC16C55, PIC16C57, PIC16CR57 12
POR
- Device Reset Timer (DRT) 31, 39
- $\overline{PD}$ 35, 41
- Power-on Reset (POR) 31, 36, 37
- $\overline{TO}$ 35, 41

PORTA 25, 36
PORTB 25, 36
PORTC 25, 36
Power-down Mode (SLEEP) 42
Prescaler 30
PRO MATE® II Universal Programmer 57
Program Counter 21

Q

Q cycles 13
Quick-Turnaround-Production (QTP) Devices 7

R

RC Oscillator 34
Read Only Memory (ROM) Devices 7
Read-Modify-Write 26
Register File Map
- PIC16C54, PIC16CR54, PIC16C55, PIC16C56, PIC16CR56 16
- PIC16C57/CR57 17
- PIC16C58/CR58 17

Registers
- Special Function 18

RESET 35
Reset 31
RESET on Brown-out 41

S

Serialized Quick-Turnaround-Production (SQTP) Devices 7
SLEEP 31, 42
Software Simulator (MPLAB-SIM) 56
Special Features of the CPU 31
Special Function Registers 18
Stack 22
STATUS 36
STATUS Register 9, 19

T

Timer0
- Switching Prescaler Assignment 30
- Timer0 (TMR0) Module 27
- TMR0 with External Clock 29

Timing Diagrams and Specifications 68, 88, 99, 122
Timing Parameter Symbology and Load Conditions 67, 87, 98, 121
TMR0 36
TRIS 36
TRIS Registers 25

U

UV Erasable Devices 7

W

W Register 36
Wake-up from SLEEP 42
Watchdog Timer (WDT) 31, 39
- Period 39
- Programming Considerations 39

WWW, On-Line Support 4

Z

Zero bit 9

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PIC16C5X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX
Device	Temperature Range	Package	Pattern

Device	PIC16C5X[2], PIC16C5XT[3] PIC16LC5X[2], PIC16LC5XT[3] PIC16CR5X[2], PIC16CR5XT[3] PIC16LCR5X[2], PIC16LCR5XT[3] PIC16LV5X[2], PIC16LV5XT[3]	
Temperature Range	b[1]	= 0°C to +70°C (Commercial)
	I	= -40°C to +85°C (Industrial)
	E	= -40°C to +125°C (Automotive)
Package	JW	= Windowed CERDIP
	P	= PDIP
	SO	= SOIC (Gull Wing, 300 mil body)
	SP	= Skinny PDIP (28-pin, 300 mil body)
	SS	= SSOP (209 mil body)
Pattern	3-digit Pattern Code for QTP, ROM (blank otherwise)	

Examples:

a) PIC16C54A -04/P 301 = Commercial temp., PDIP package, 4MHz, normal VDD limitis, QTP pattern #301.

b) PIC16LC58A - 04I/SO = Industrial temp., SOIC package, 4MHz, Extended VDD limits.

c) PIC16CR54A - 10I/P355 = ROM program memory, Industrial temp., PDIP package, 10MHz, normal VDD limits.

Note 1: b = blank

2: C = Standard VDD range
LC = Extended VDD range
CR = ROM Version, Standard VDD range
LCR = ROM Version, Extended VDD range
LV = Low Voltage VDD range

3: T = in tape and reel - SOIC, SSOP packages only.

4: UV erasable devices are tested to all available voltage/frequency options. Erased devices are oscillator type 04. The user can select 04, 10 or 20 oscillators by programmng the appropriate configuration bits.

PIC16C54/55/56/57 PRODUCT IDENTIFICATION SYSTEM

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PART NO.	-XX	X	/XX	XXX
Device	Oscillator Type	Temperature Range	Package	Pattern

Device	PIC16C54, PIC16C54T[2] PIC16C55, PIC16C55T[2] PIC16C56, PIC16C56T[2] PIC16C57, PIC16C57T[2]	
Oscillator Type	RC LP XT HS 10 b[1]	= Resistor Capacitor = Low Power Crystal = Standard Crystal/Resonator = High Speed Crystal = 10 MHz Crystal = No type for JW[3] devices
Temperature Range	b[1] I E	= 0°C to +70°C (Commercial) = -40°C to +85°C (Industrial) = -40°C to +125°C (Automotive)
Package	JW P S SO SP SS	= Windowed CERDIP = PDIP = Die in Waffle Pack = SOIC (Gull Wing, 300 mil body) = Skinny PDIP (28 pin, 300 mil body) = SSOP (209 mil body)
Pattern	3-digit Pattern Code for QTP (blank otherwise)	

Examples:

a) PIC16C54 - XT/PXXX = "XT" oscillator, commercial temp., PDIP, QTP pattern.

b) PIC16C55 - XTI/SO = "XT" oscillator, industrial temp., SOIC (OTP device)

c) PIC16C55 /JW = Commercial temp. CERDIP with window.

d) PIC16C57 - RC/S = "RC" oscillator, commercial temp., dice in waffle pack.

Note 1: b = blank

2: T = in tape and reel - SOIC, SSOP packages only.

3: UV erasable devices are tested to all available voltage/frequency options. Erased devices are oscillator type RC. The user can select RC, LP, XT or HS oscillators by programming the appropriate configuration bits.

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